

# SULLIVAN

REV : X01

@ : Depop Component for All

Dothan Schematic with Capture CIS and Function field

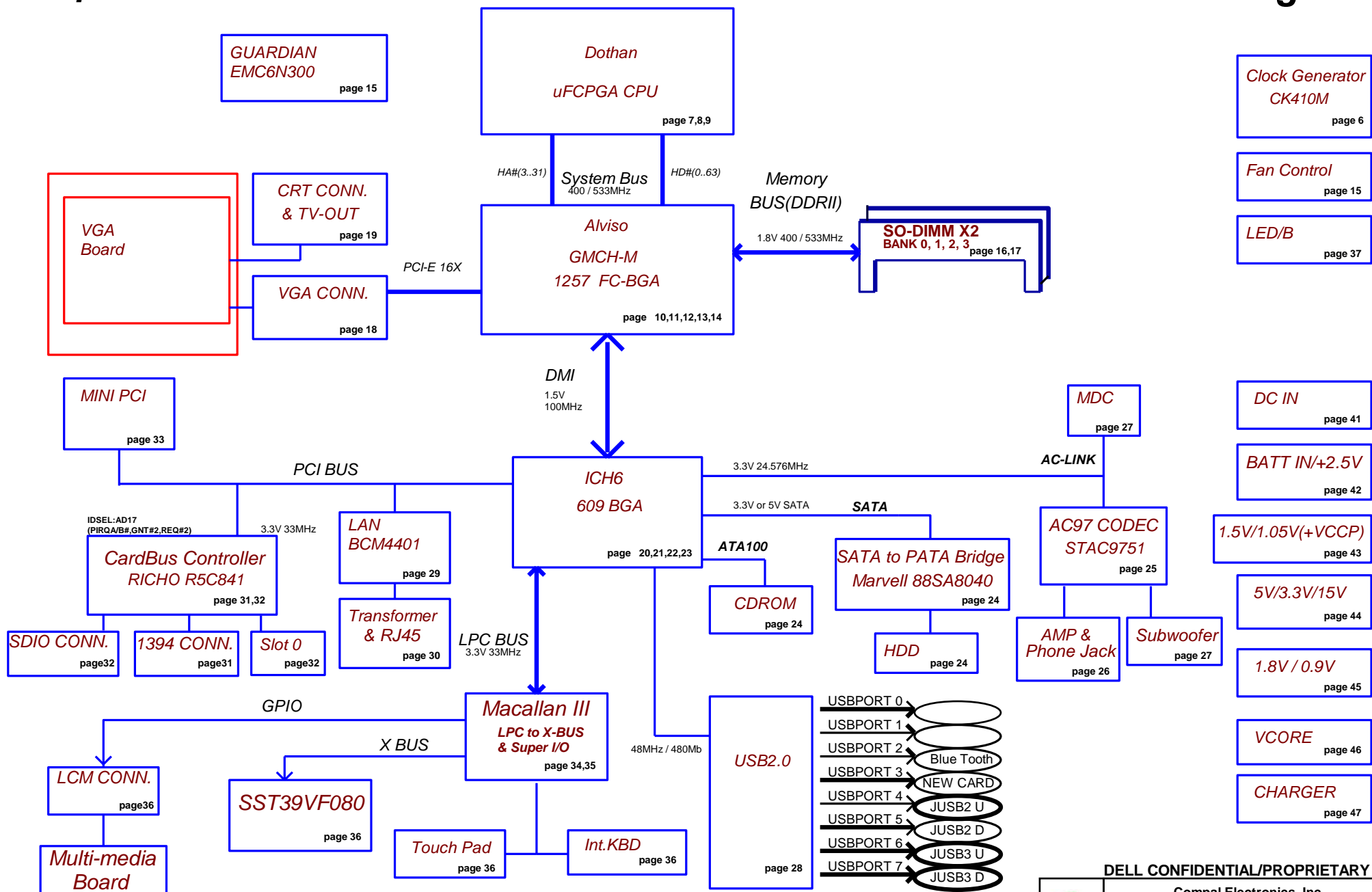
uFCPGA Dothan  
02-11-2004  
REV: 0.2

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Compal Electronics, Inc.



Title			Cover Sheet	
Size	Document Number	Rev		
	LA-2171	0.2		
Date	12/2004	Sheet	1	of 50



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Block Diagram

Size	Document Number	Rev
	LA-2171	0.2

Date: 12, 2004 Sheet: 2 of 50

PM TABLE

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
MINI PCI	AD19	3	D,B
LAN	AD16	4	C

USB TABLE

USB PORT#	DESTINATION
0	
1	
2	Blue Tooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	
7	

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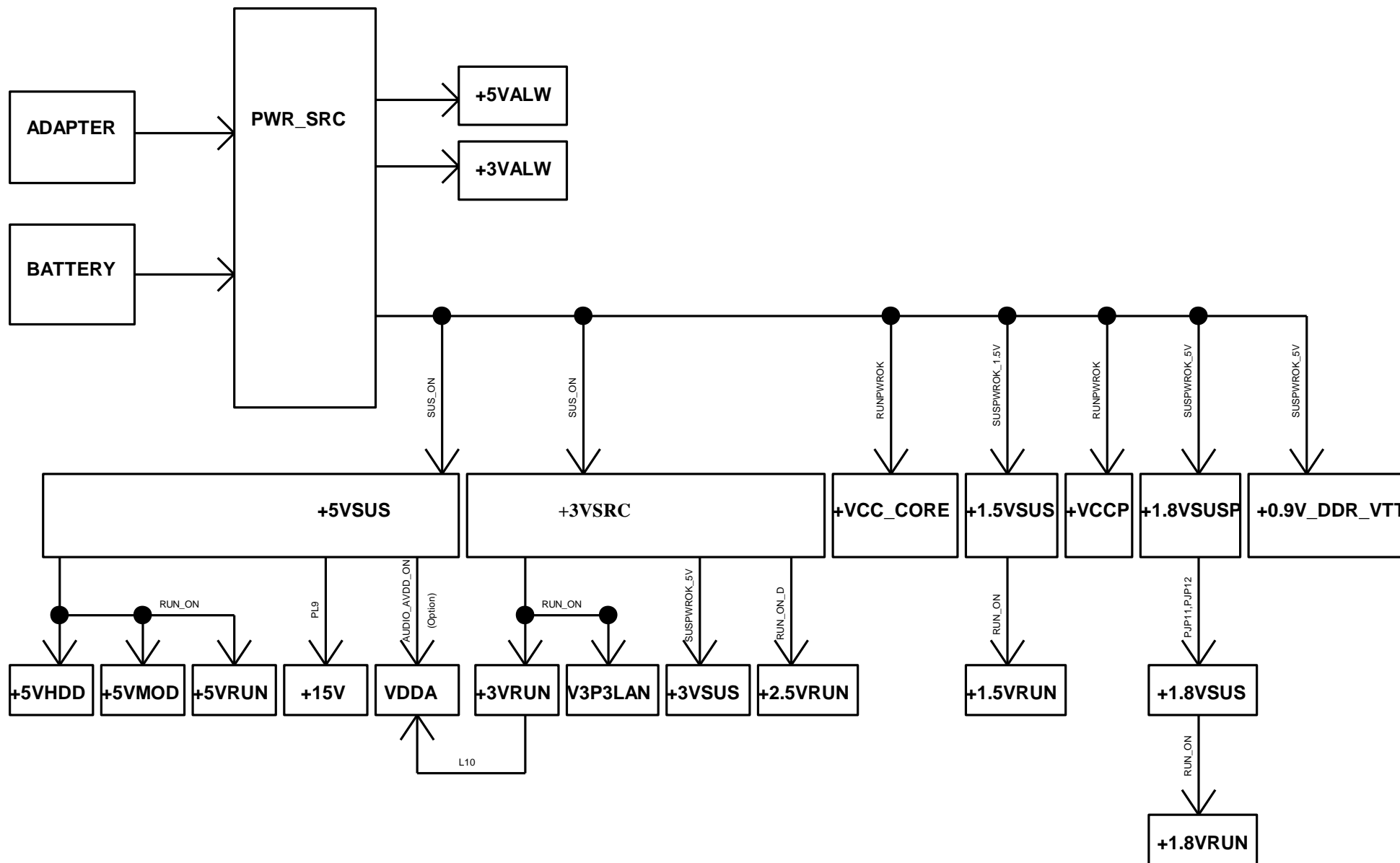
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Index and Config.



Size	Document Number	Rev
	LA-2171	0.2

Date: 12/2004 Sheet 3 of 50



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Power Rail

Size Document Number

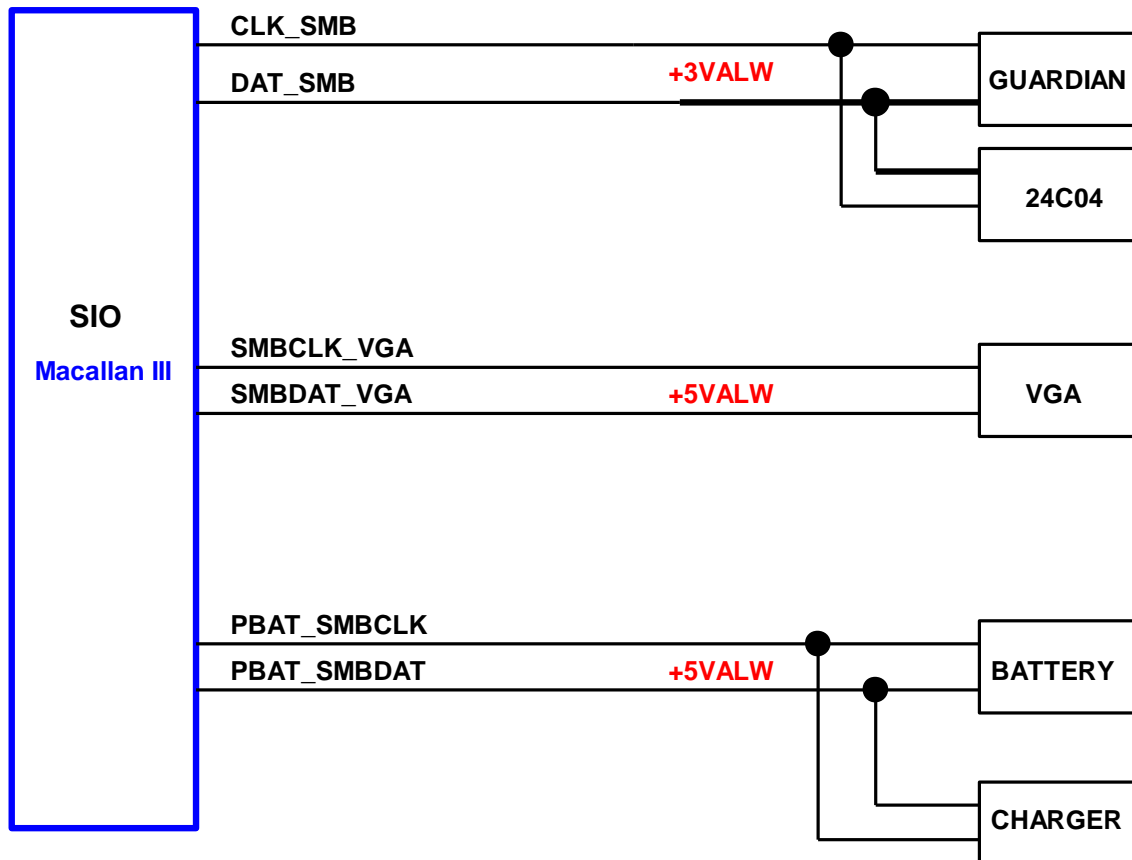
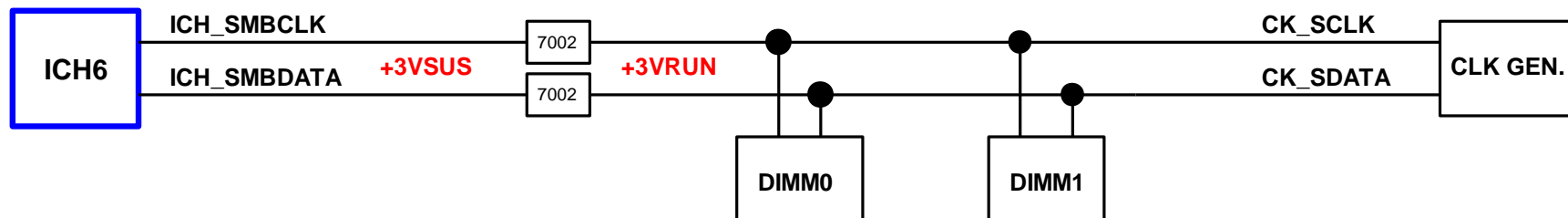
LA-2171

Rev

0.2

Date 12/2004

Sheet 4 of 50



Device	Address
DIM0	A0h
DIM1	A2h
CLK GEN.	D2h
GUARDIAN	5Eh
24C04	A2h
VGA	58h
Battery	16h
Charger	12h

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SMBUS TOPOLOGY

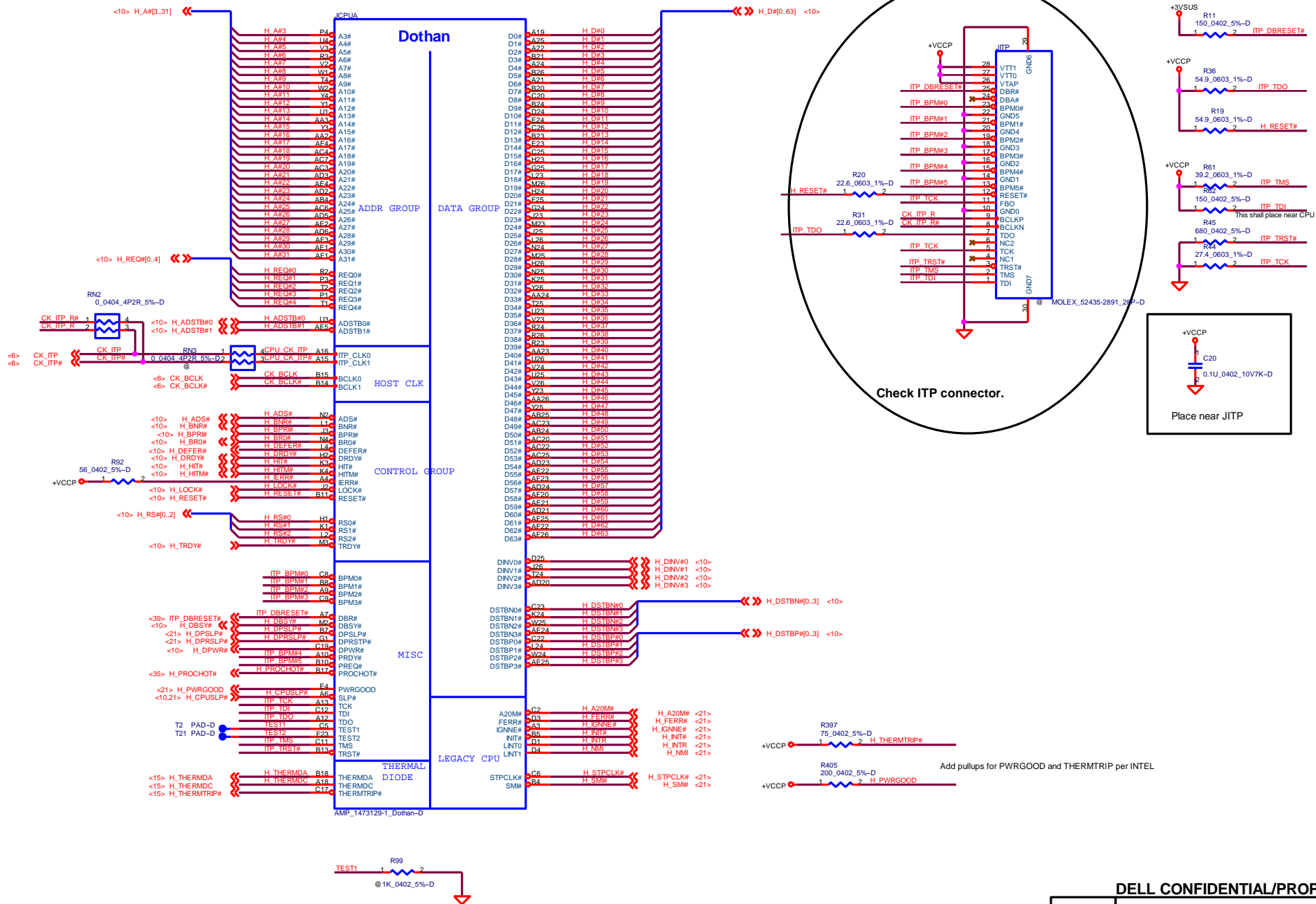
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Date 12/2004 Sheet 5 of 50 Rev 0.2



Date: 12, 2004 Sheet 6 of 50

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Dothan Processor(1/2)

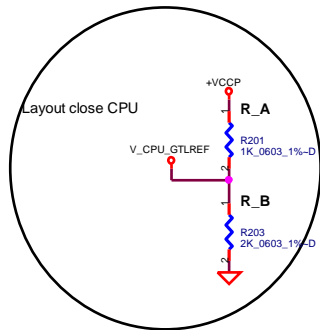
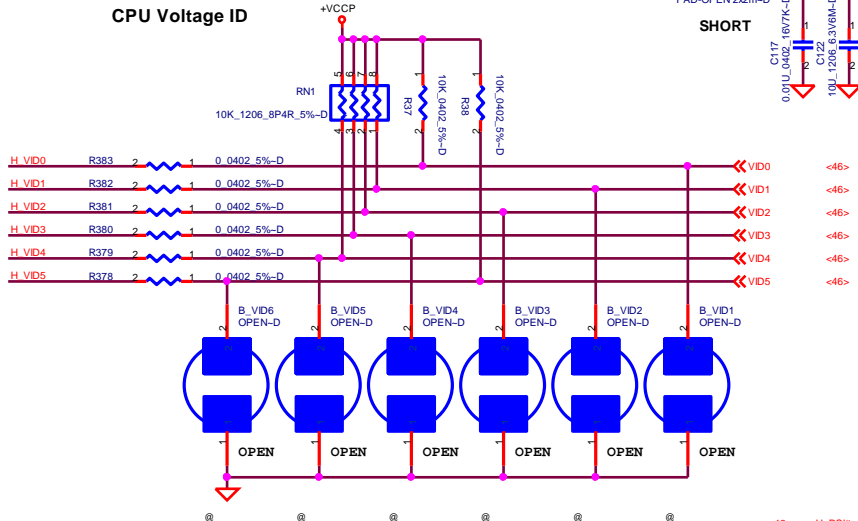
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Rev 0.2

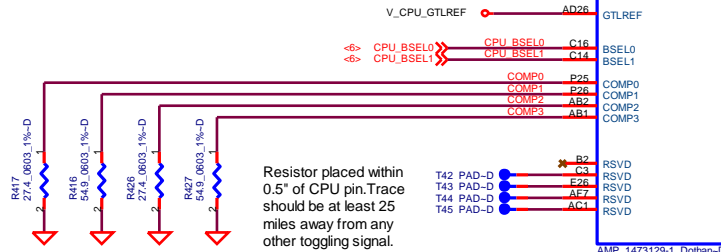
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For test only ,Cmos output



**Layout Note:**  
500 mil max length



**Dothan**

POWER, GROUND, RESERVED SIGNALS AND NC

**Dothan**

POWER, GROUND

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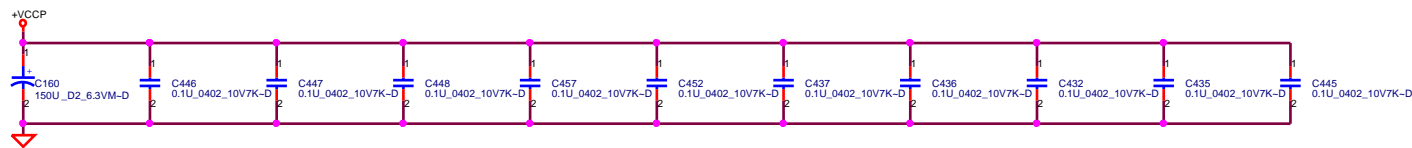
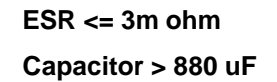
Dothan Processor(2/2)

LA-2171

12, 2004

Sheet 8 of 50

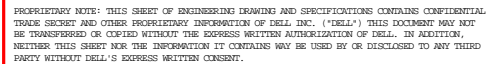
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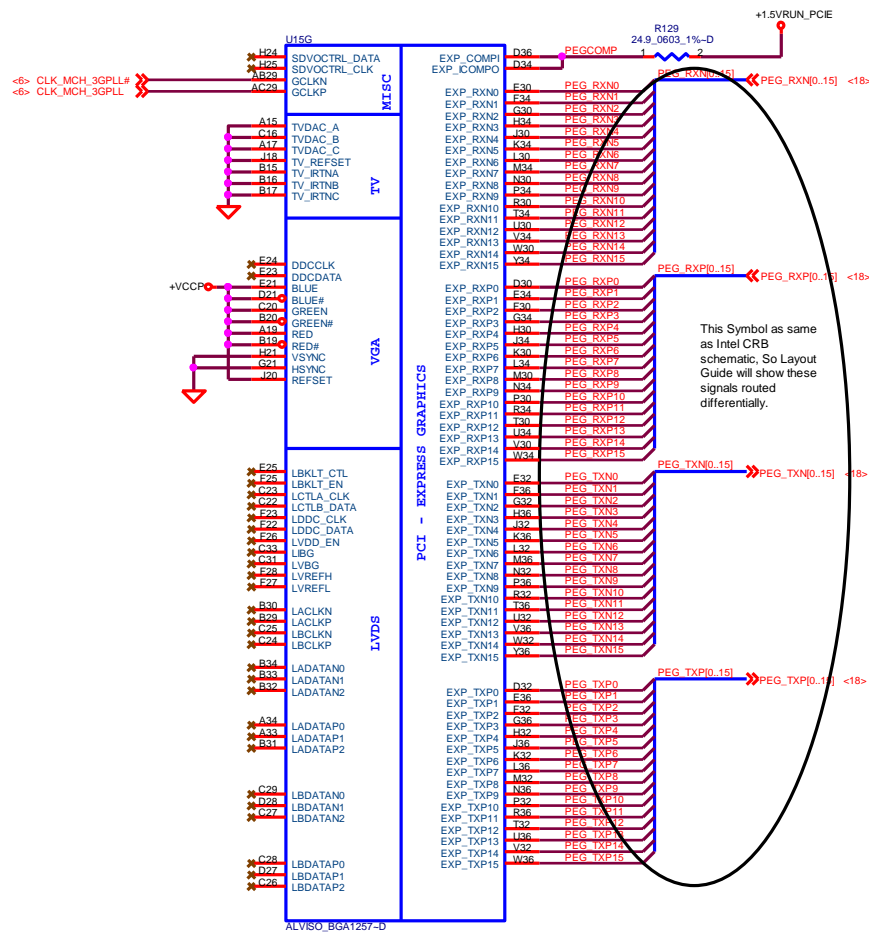


Date: 12.2004 Sheet 9 of 50

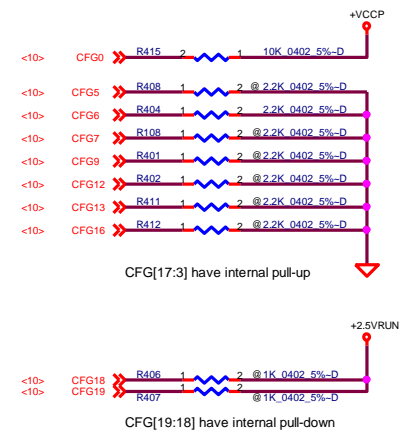
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CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XDR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



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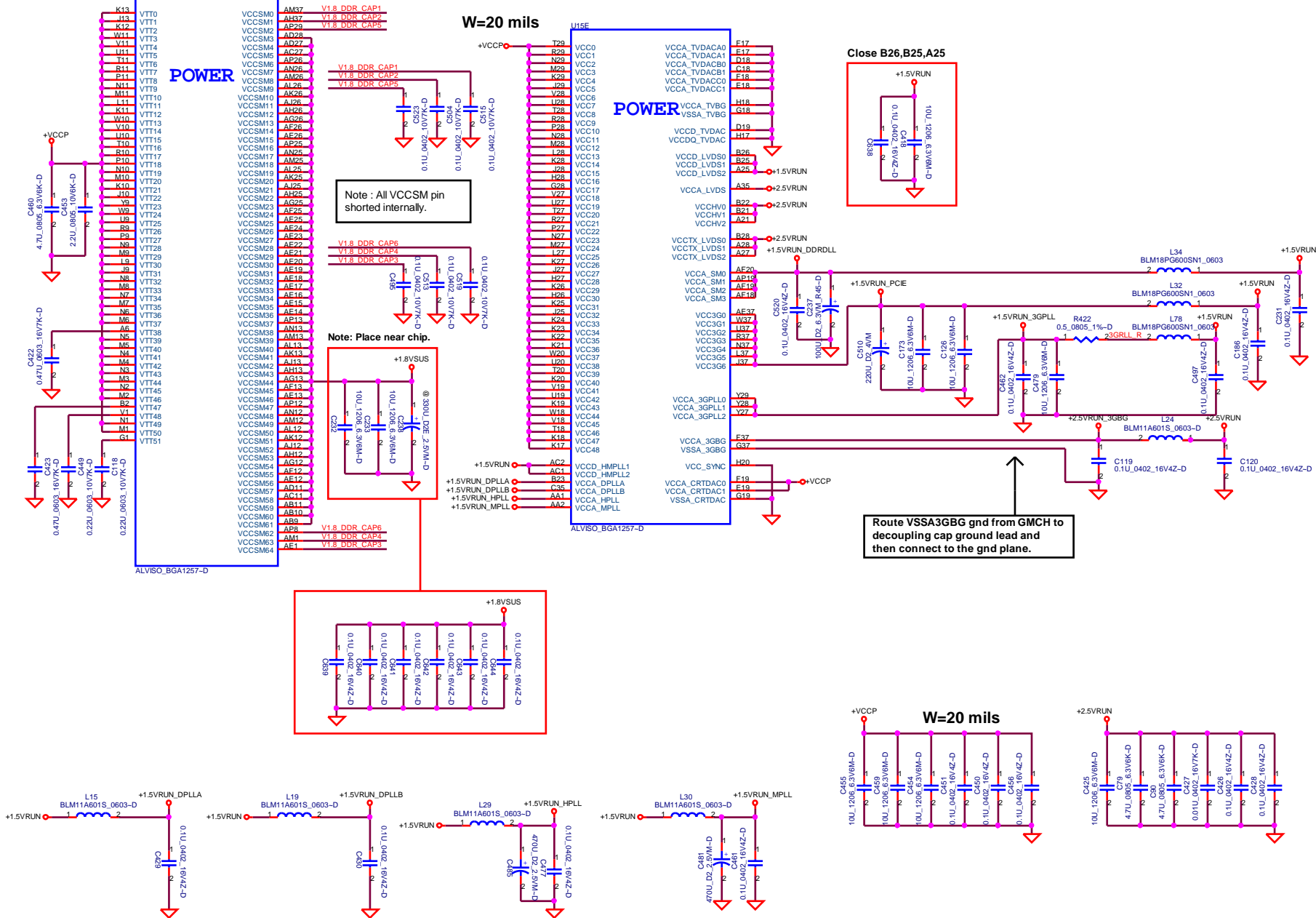


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Alviso(3 of 5)

Size	Document Number	Rev
LA-2171		0.2
Date	12/2004	Sheet 12 of 50



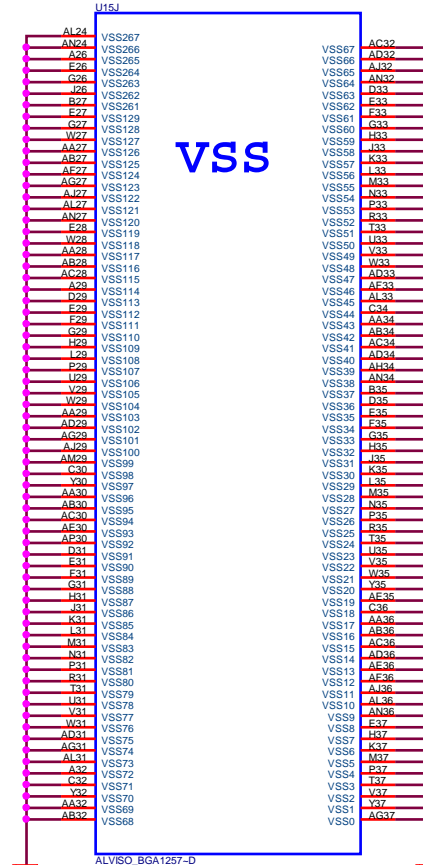
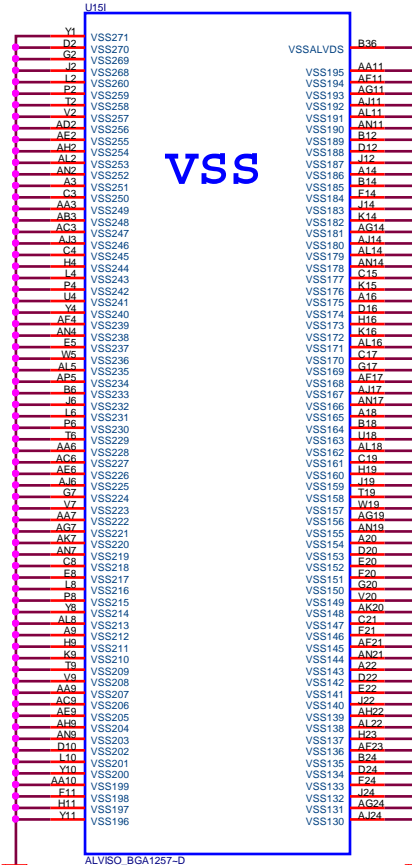
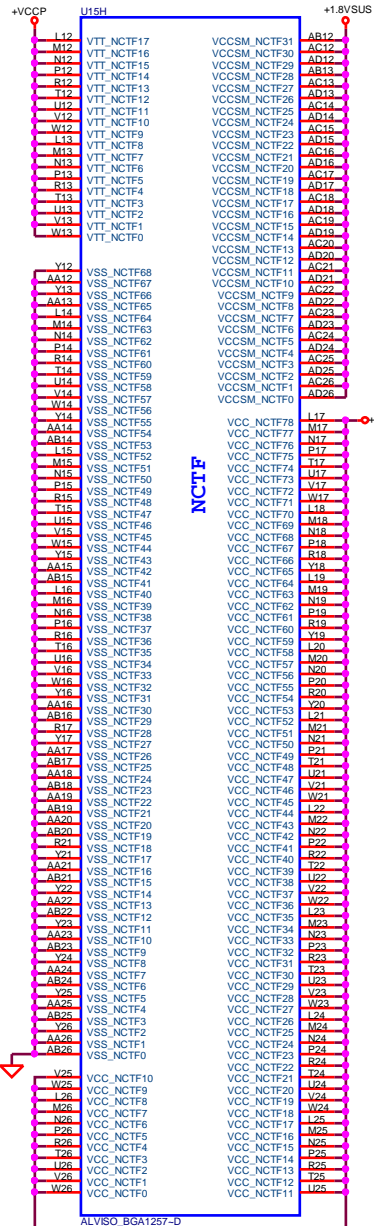
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Alviso(4 of 5)

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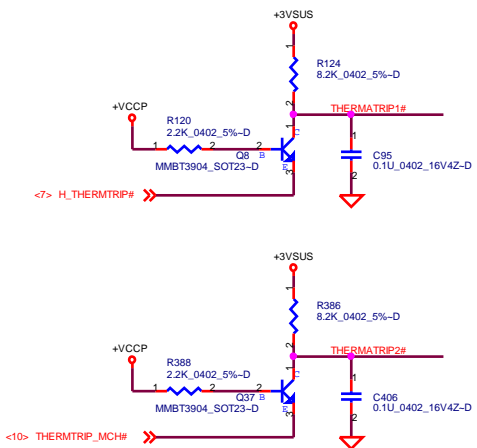
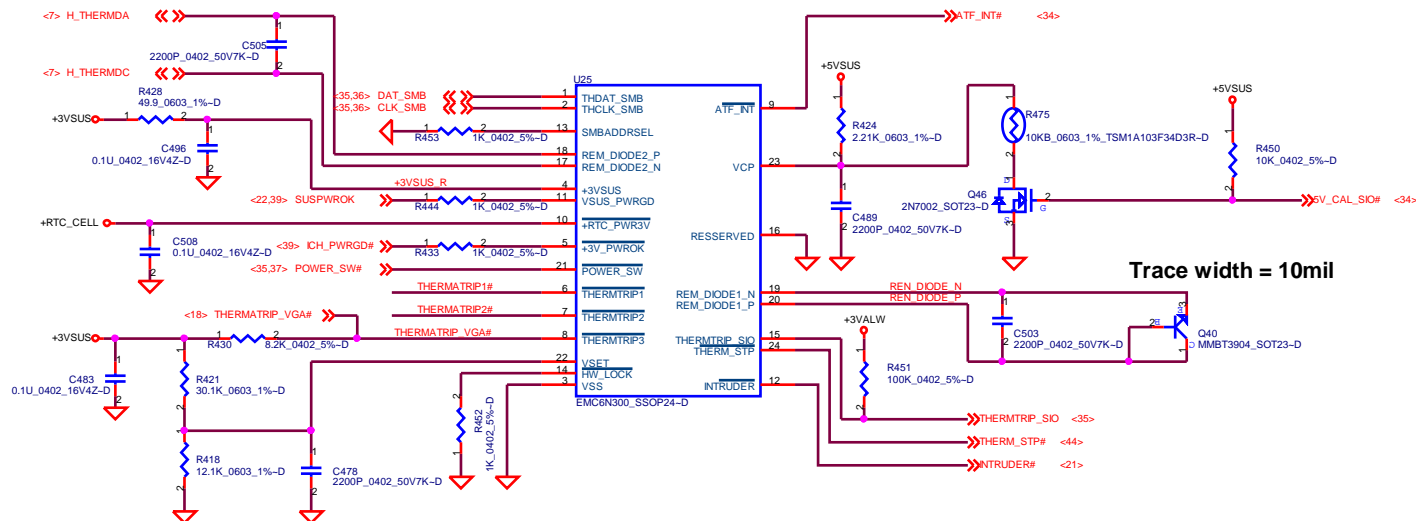
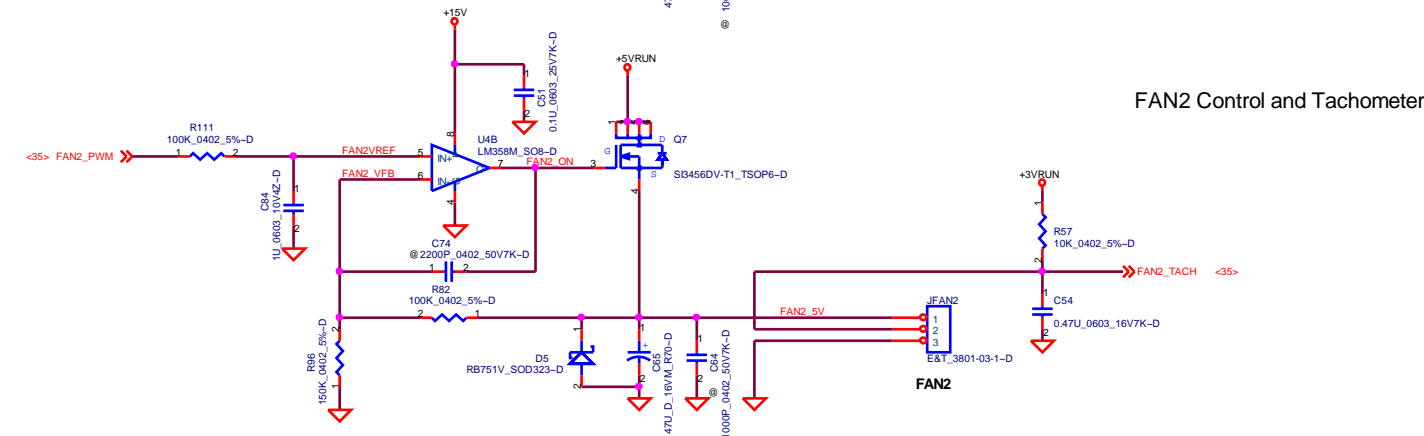
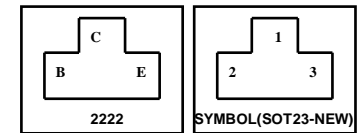
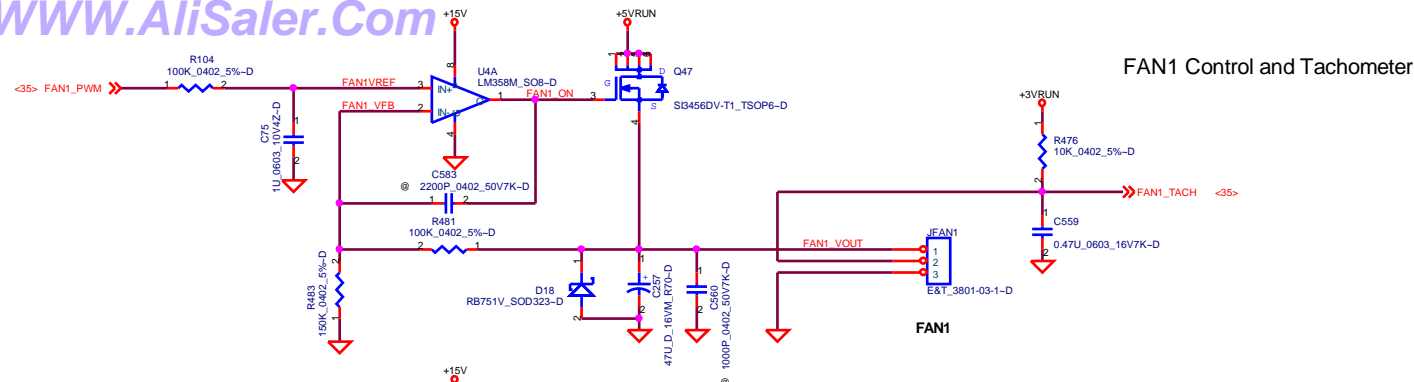
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Alviso(5 of 5)

Size Document Number LA-2171 Rev 0.2

Date 12/2004 Sheet 14 of 50

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Thermal sensor and Fan

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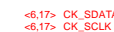
Date 12, 2004 Sheet 15 of 50

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A schematic diagram showing a 10pF capacitor, labeled C287, connected between two signal lines. The top signal line is labeled M\_CLK\_DDR#3 and the bottom signal line is also labeled M\_CLK\_DDR#3. The capacitor is represented by two parallel blue lines. The value 10P\_0402\_50V8 is indicated near the capacitor.

The diagram shows a power distribution network for DDR VTT. A +0.9V supply is connected to a series of capacitors (C580 to C596) which are connected to a common ground. Each capacitor is labeled with its value: 0.1u, 0.0402, 16V4Z-D.

**Layout Note:**  
Place these resistor  
closely JDIM1,all  
trace length  
Max=1.3"



## DIMMA STANDARD

Rev	0.2
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The diagram shows a capacitor labeled C328. One terminal of the capacitor is connected to a power supply labeled 10P\_0402\_50V8U-D. The other terminal is connected to a signal line labeled M\_CLK\_DDR0. The signal line is also labeled M\_CLK\_DDR#0 at the bottom right.

10.0V\_DDR\_VTT

0.1U,0A02,,18V4Z-D

C3060

0.1U,0A02,,18V4Z-D

C3061

0.1U,0A02,,18V4Z-D

C3062

0.1U,0A02,,18V4Z-D

C3063

0.1U,0A02,,18V4Z-D

C3064

0.1U,0A02,,18V4Z-D

C3065

0.1U,0A02,,18V4Z-D

C3066

0.1U,0A02,,18V4Z-D

C3067

0.1U,0A02,,18V4Z-D

C3068

0.1U,0A02,,18V4Z-D

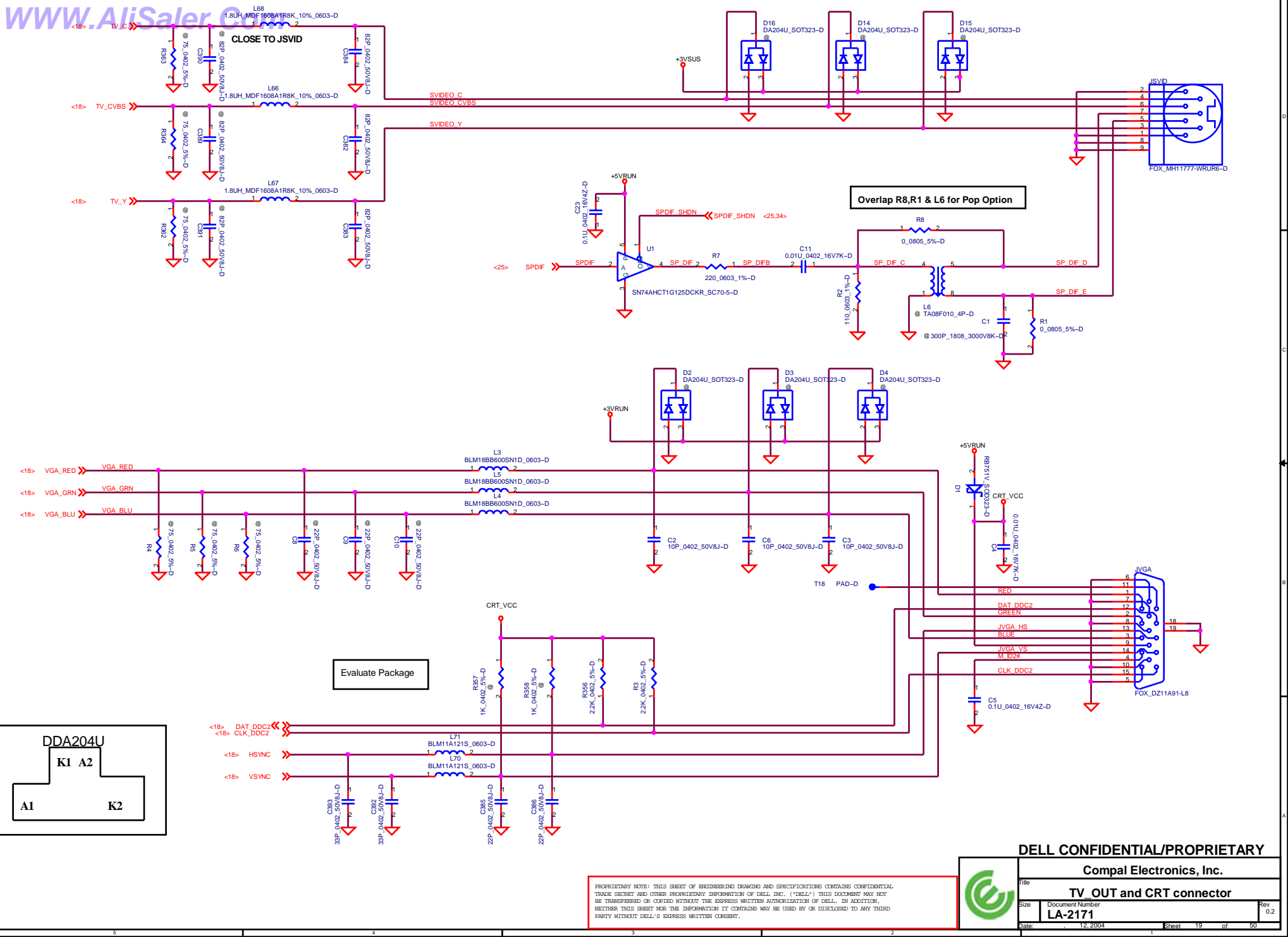
C3069

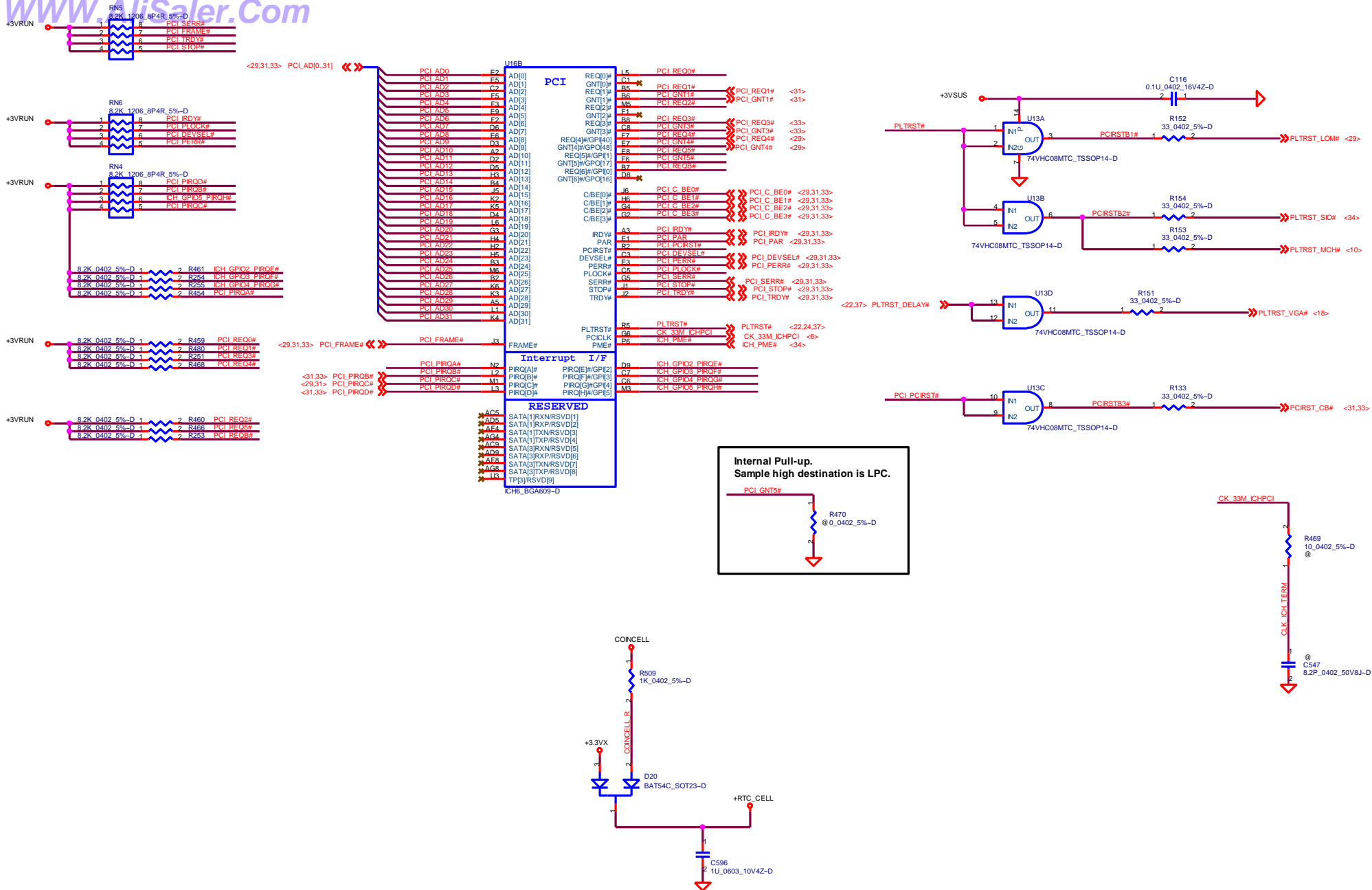
**Layout Note:**  
Place these resistor  
closely JDIM2,all  
trace length Max=1.3

**DIMMB  
REVERSE**

Rev  
02







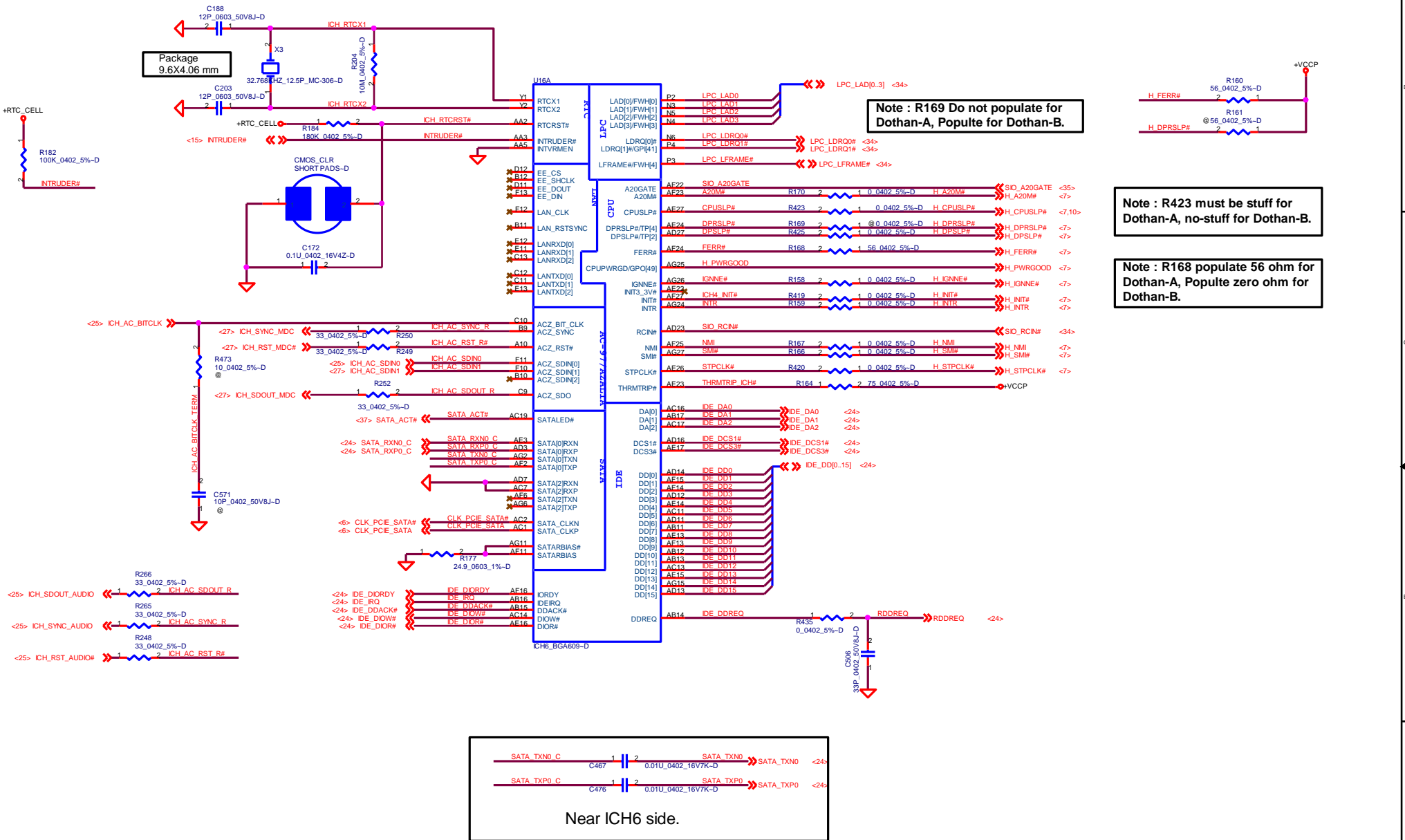
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Size	Document Number
	LA-2171

Date: 12.2004 Sheet 20 of 50



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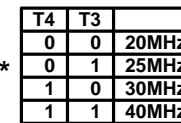


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Size	Document Number	Rev	
LA-2171		0.2	
Date	12/2004	Sheet	21 of 50

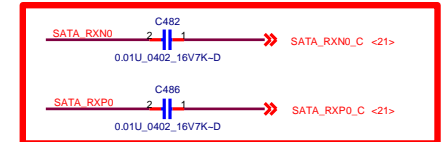


Date: 12, 2004 Sheet 22 of 50

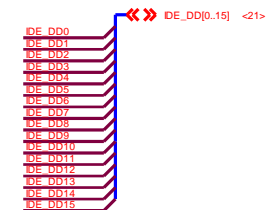




Pin Name	Pin No.	Int. PU/PD	Settings
SAYATEST0	33	PD	NC
SAYATEST1	34	PU	NC
SAYATEST2	35	PD	NC
SAYATEST3	36	PD	1
SAYATEST4	37	PD	NC
SAYATEST5	38	PU	0
SAYATEST6	39	PD	1
SAYATEST7	40	PD	NC
CFG0	20	PD	NC
CFG1	19	PU	0
CFG2	18	PD	NC

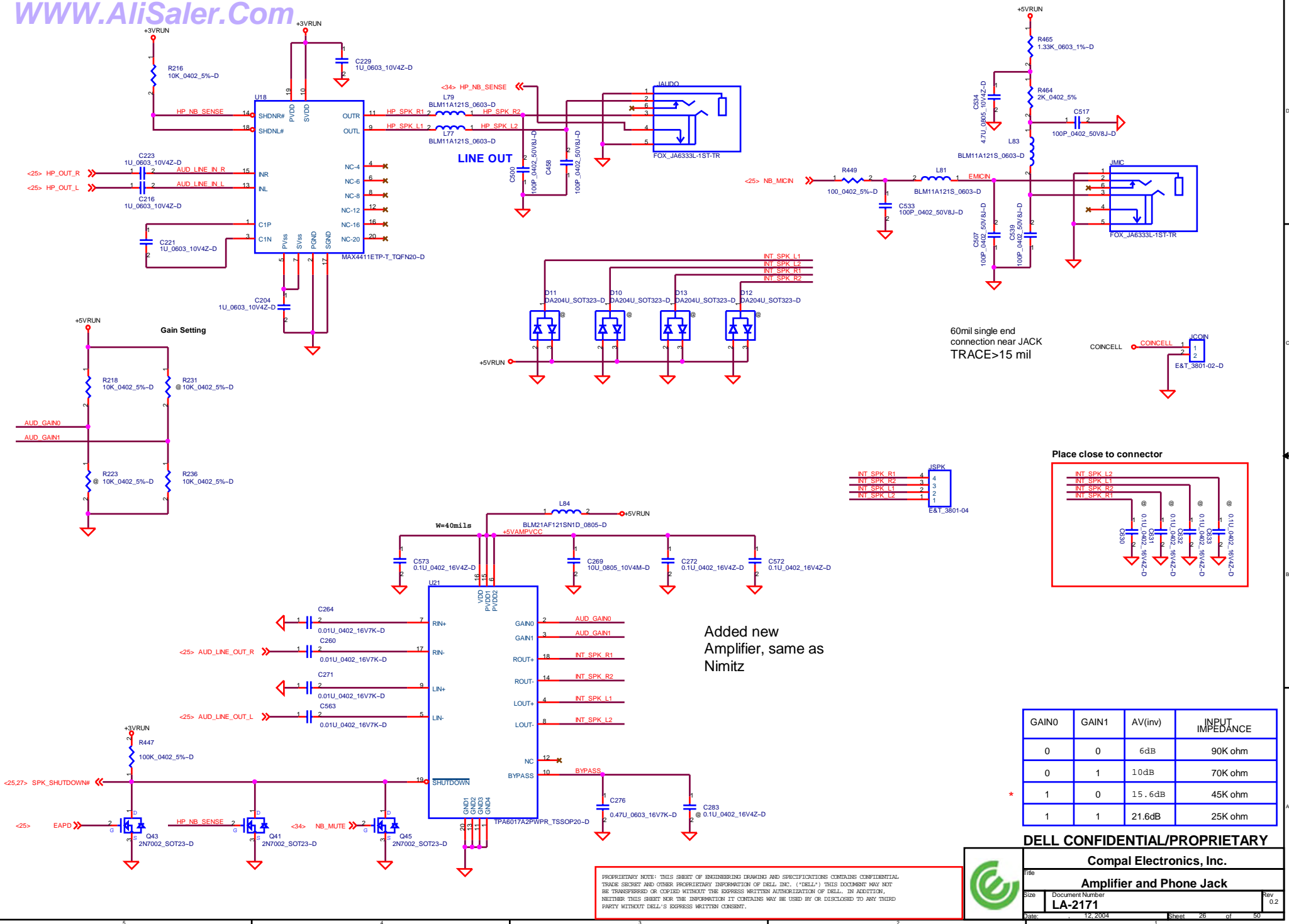


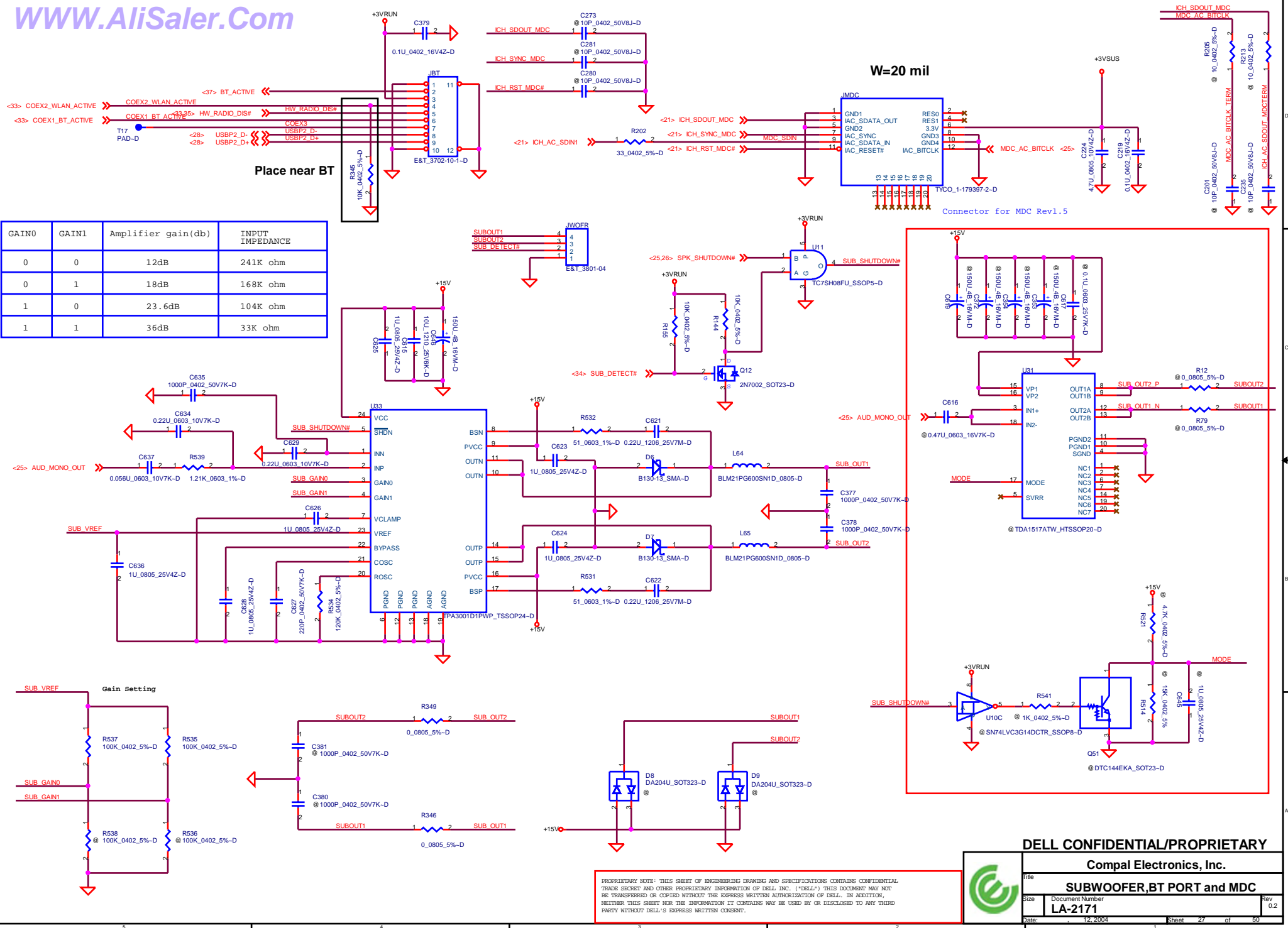
<21> IDE\_DDACK# >> 1 2 RPDDACK#  
22\_0402\_5%~D

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Size	Document Number <b>LA-2171</b>	Rev 0.2
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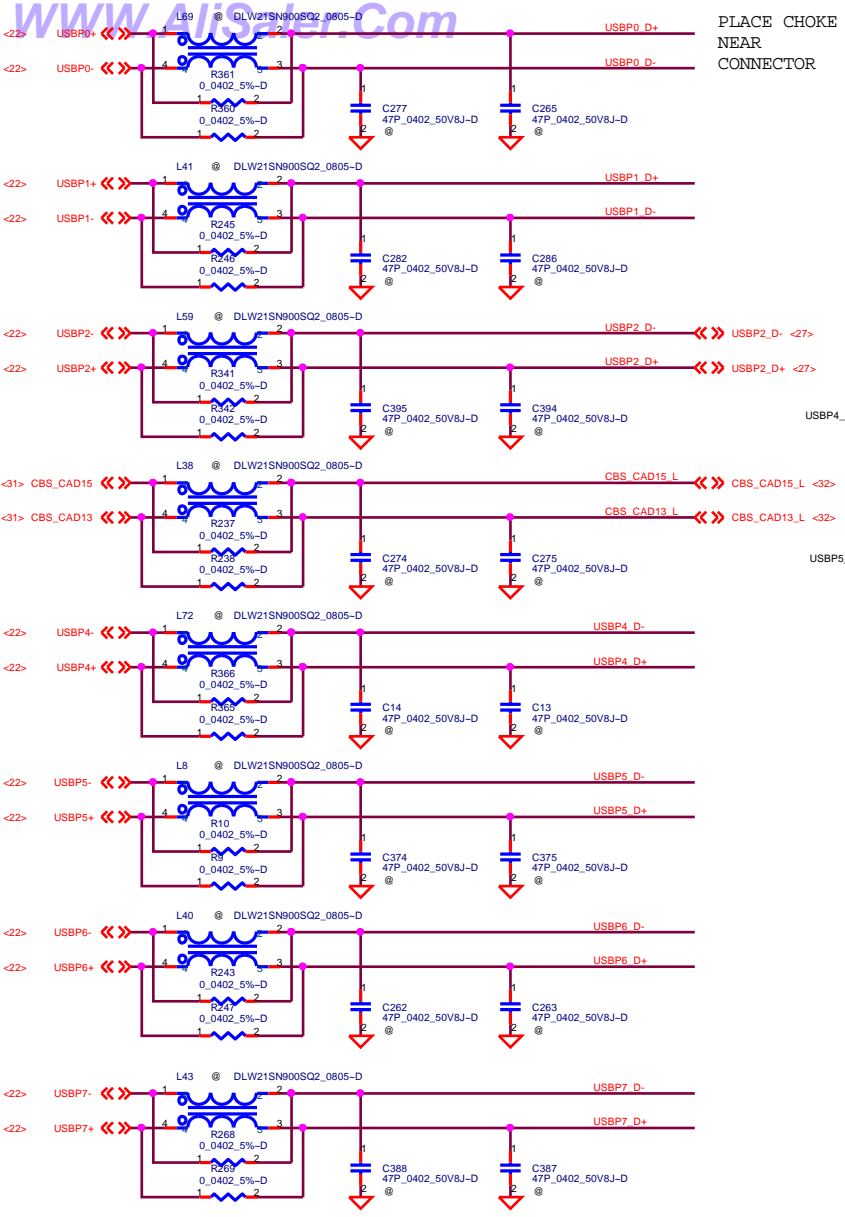




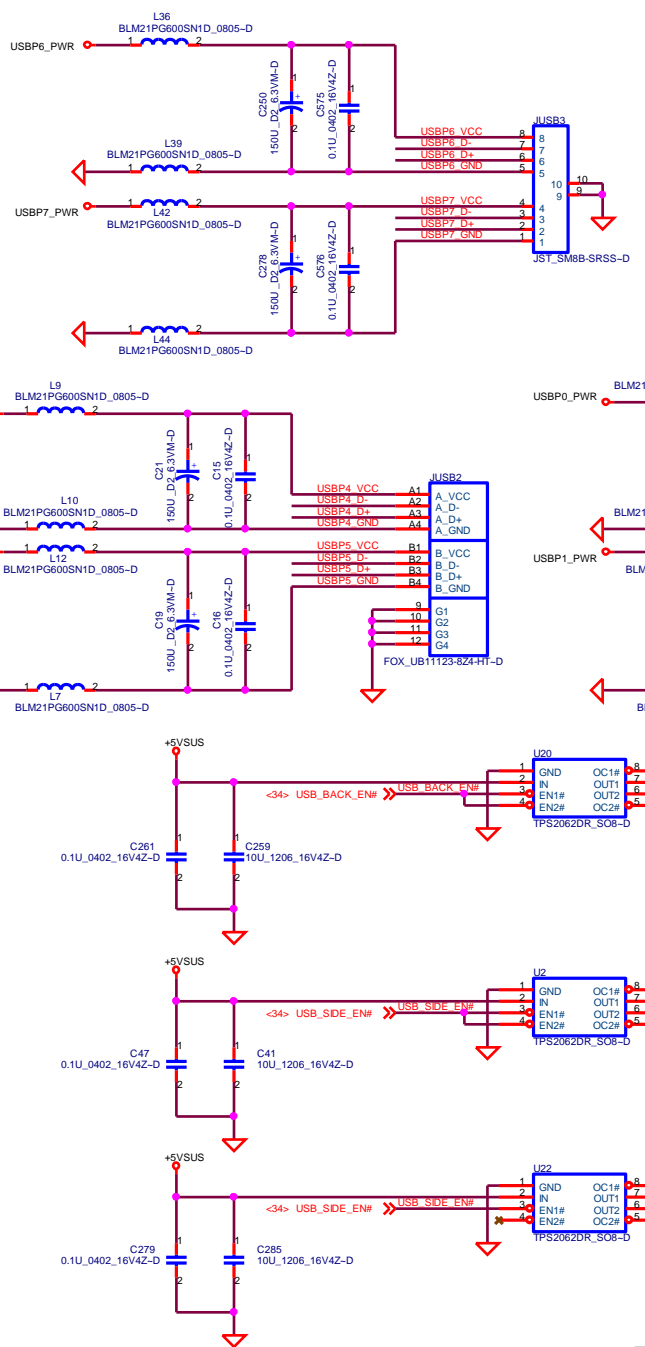
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Size	Document Number	Rev	
	LA-2171	0.2	
Date	12, 2004	Sheet	27 of 50



PLACE CHOKE  
NEAR  
CONNECTOR



USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	BlueTooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)

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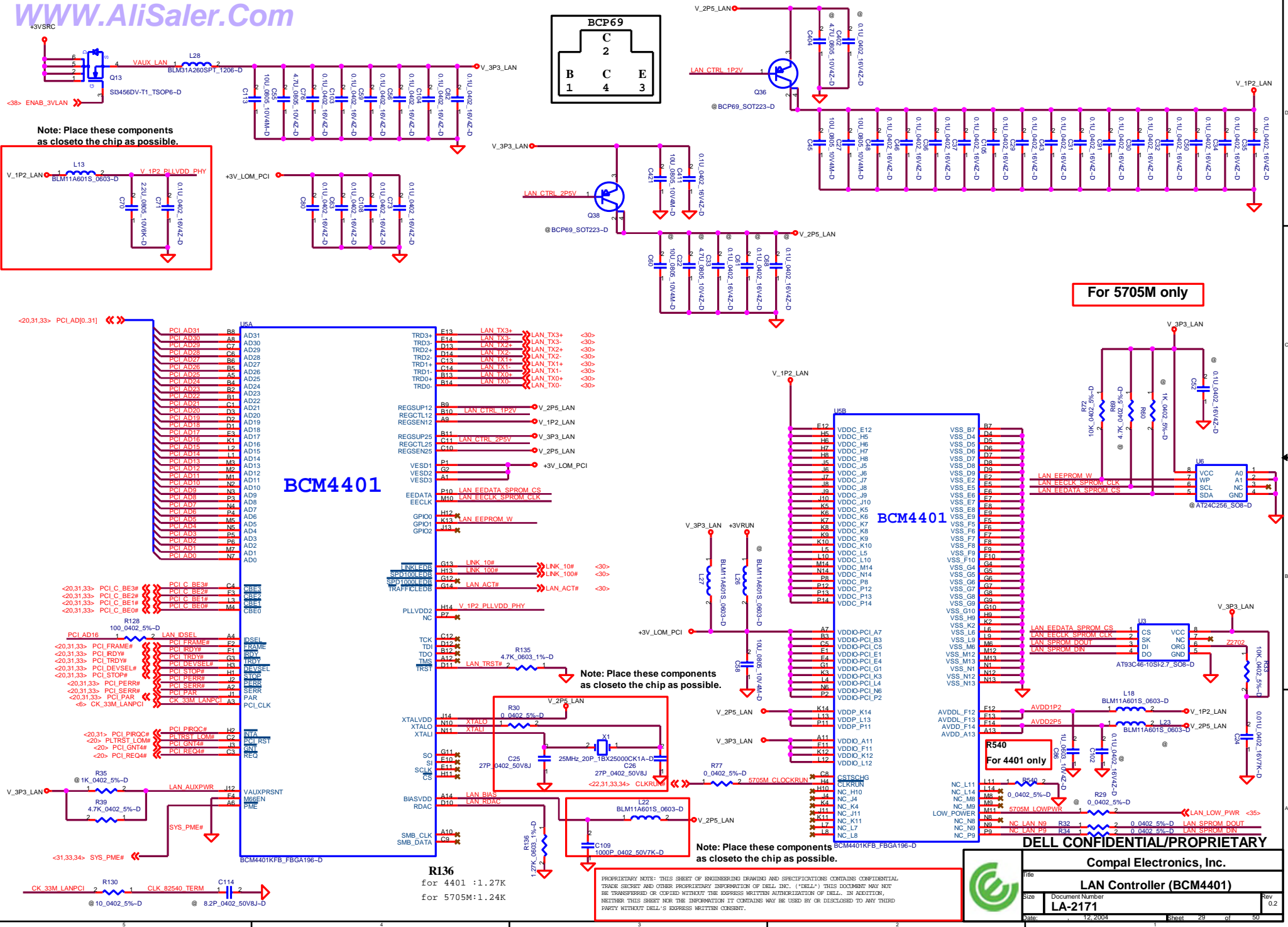
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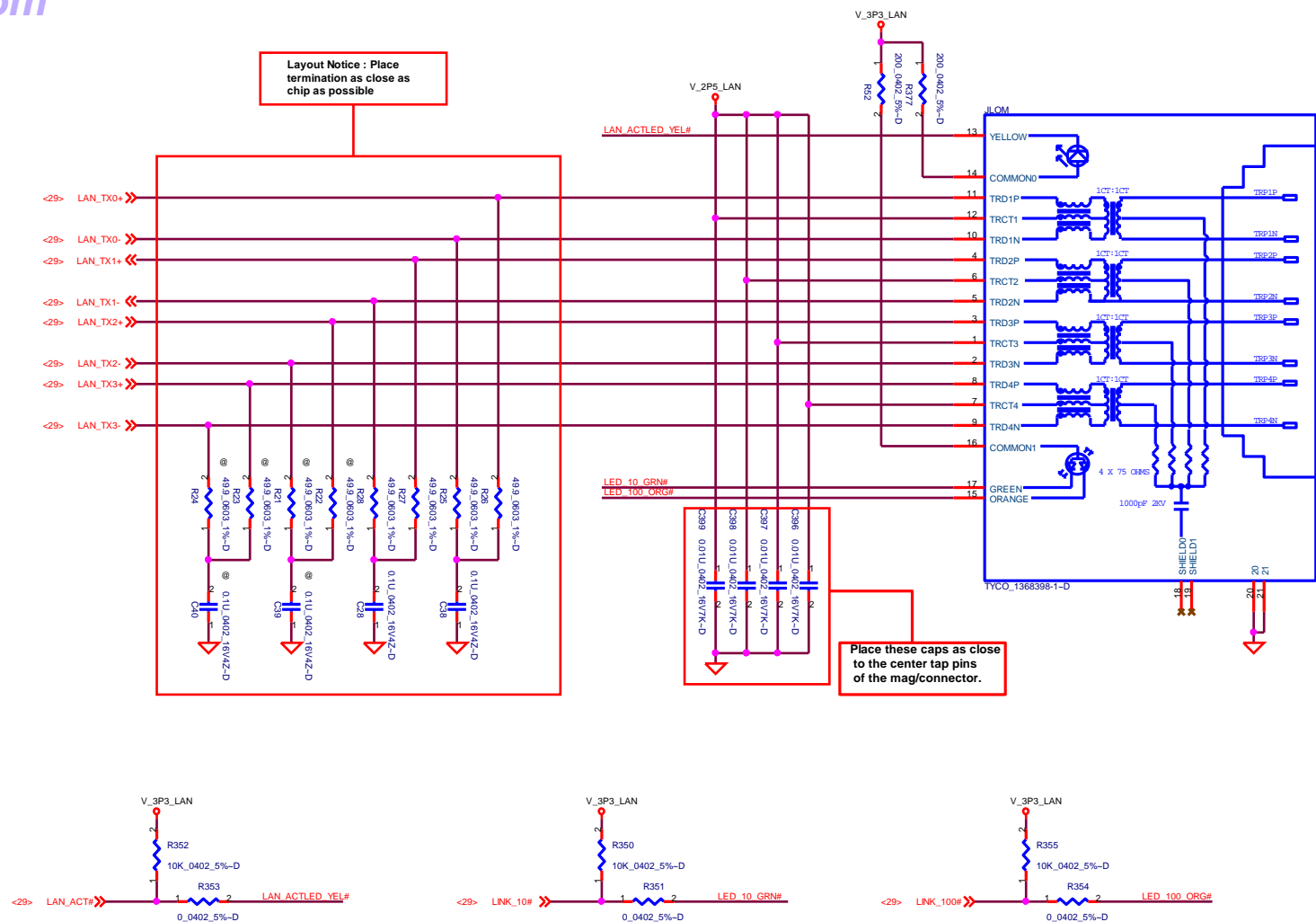
USB 2.0 PORT

LA-2171

Size 12, 2004 Sheet 28 of 50

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LAN Transfomer and RJ45

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LA-2171

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Sheet

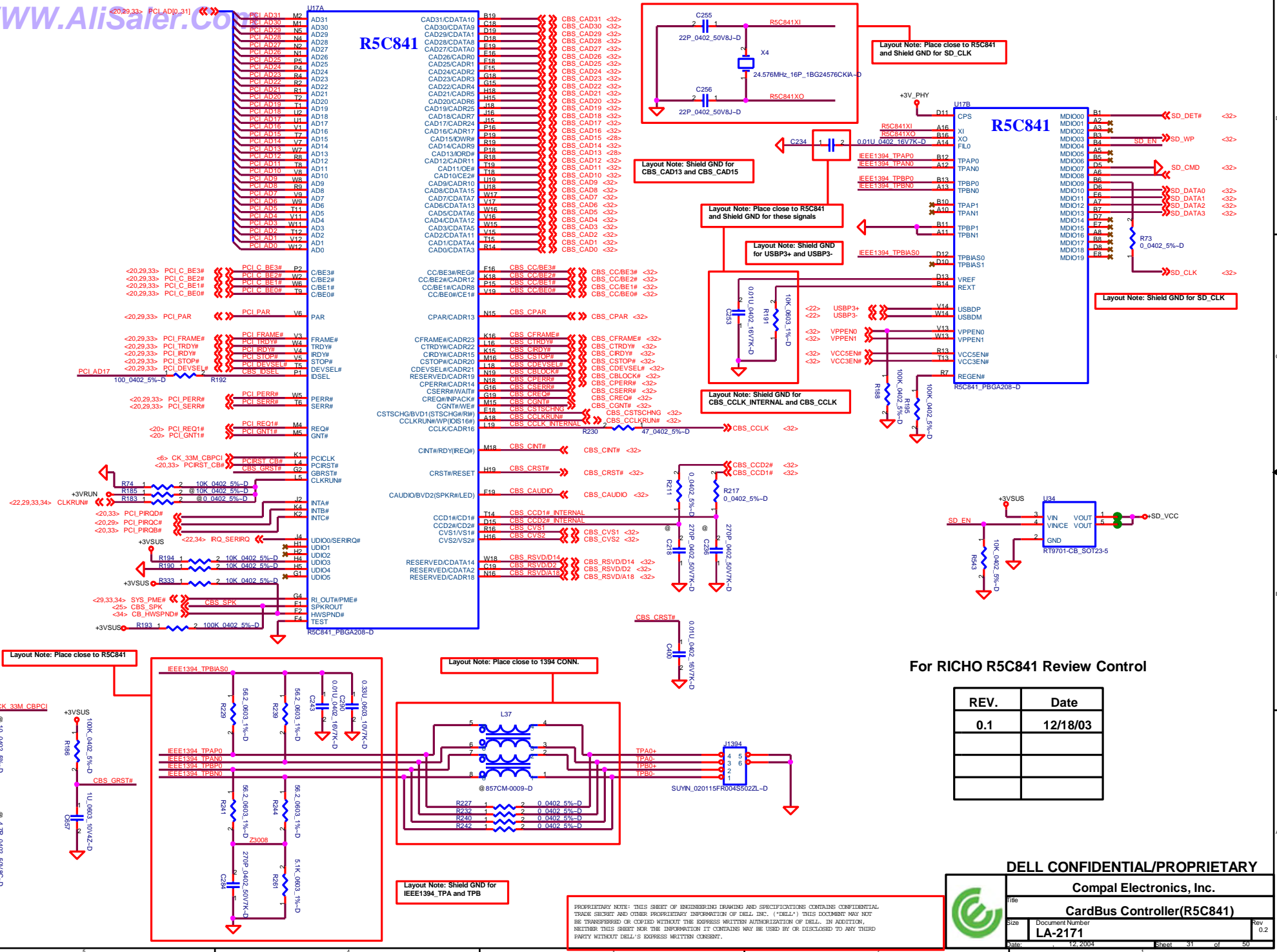
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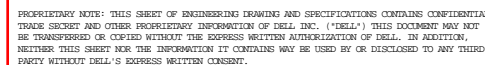
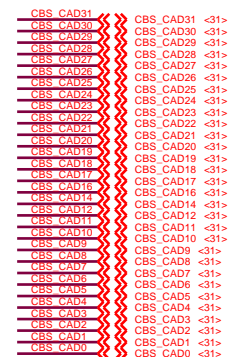
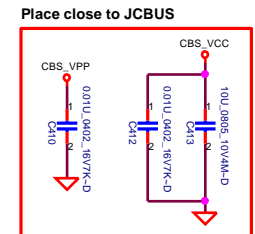
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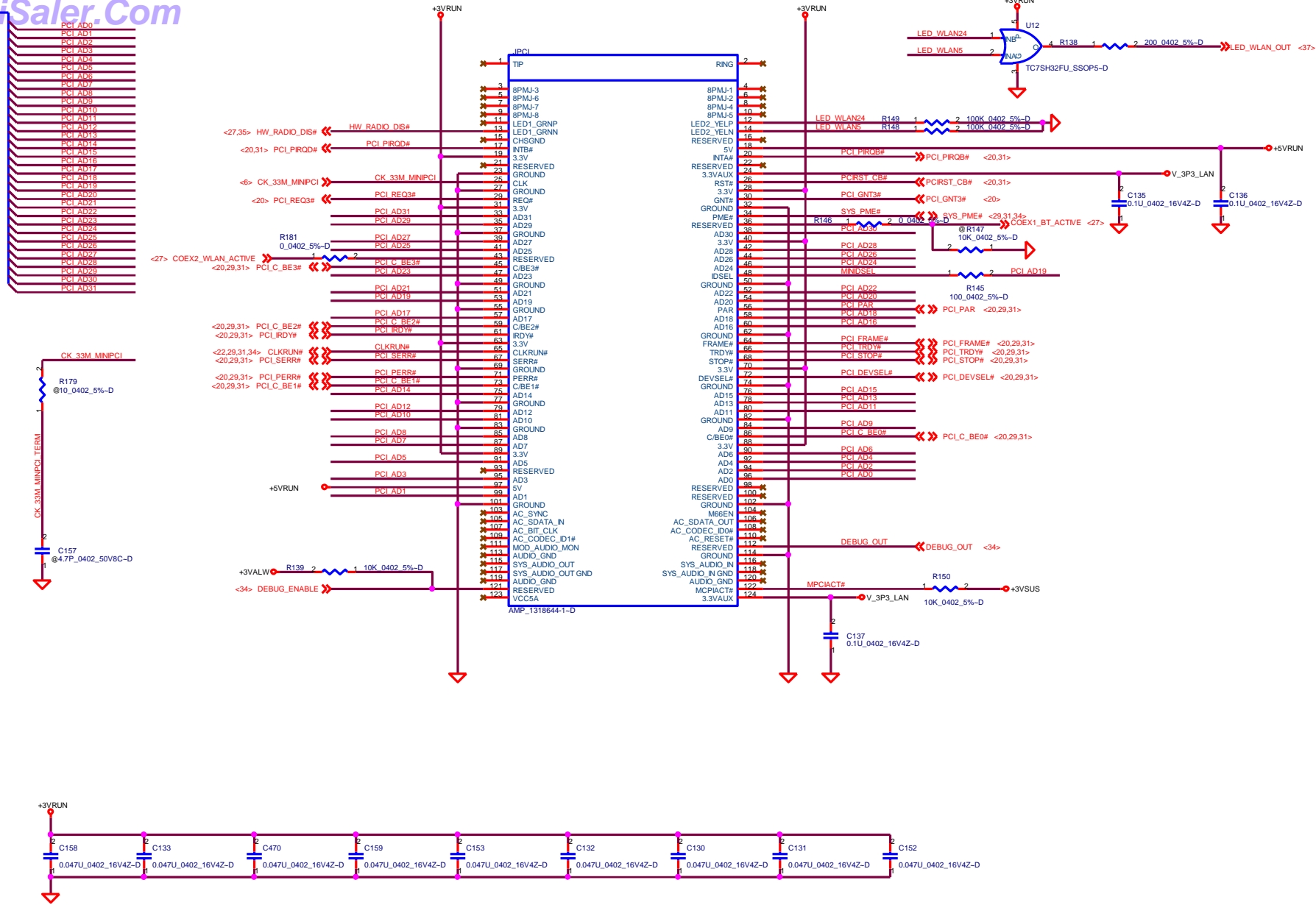
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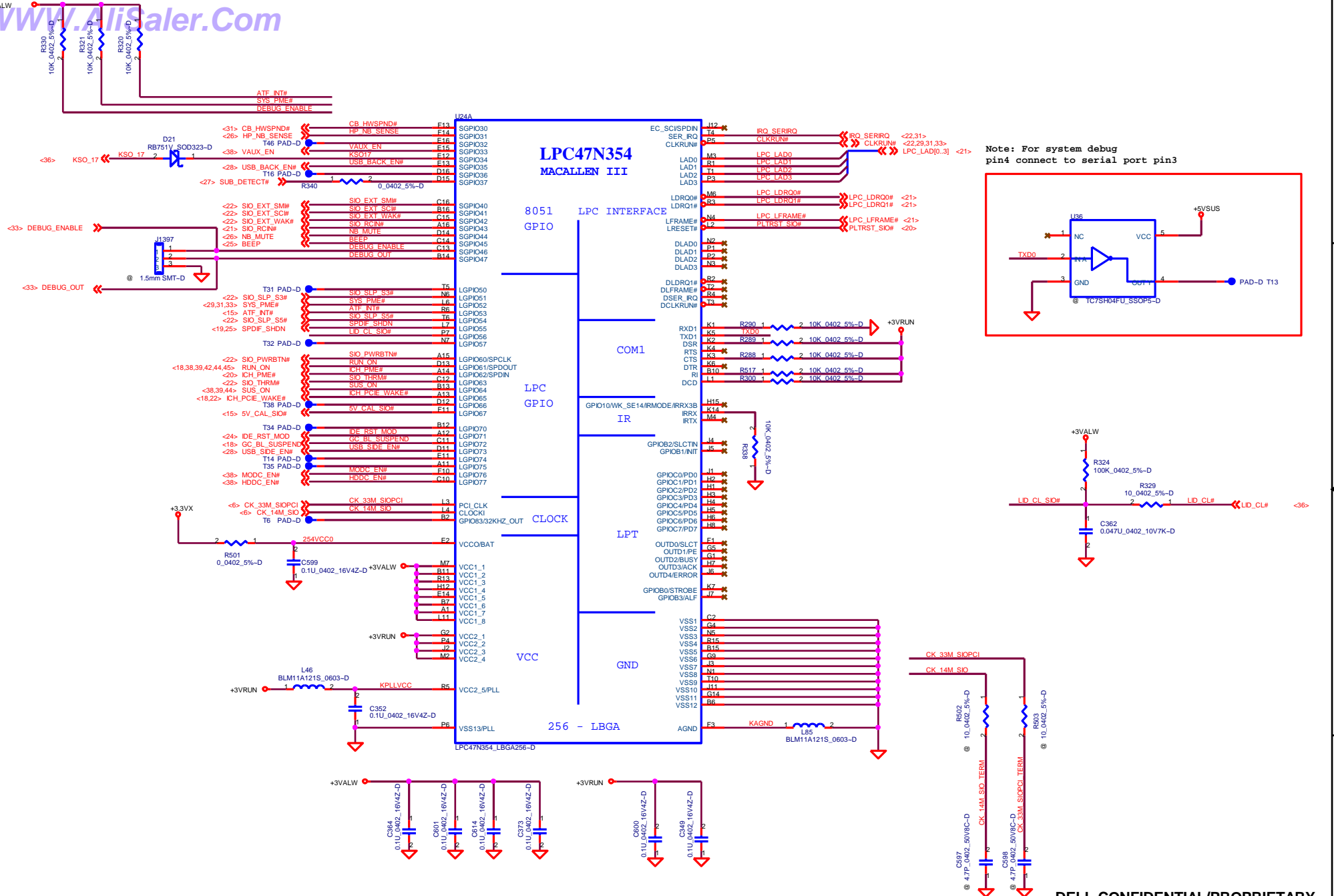
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Document Number  
**LA-2171**

Rev  
0.2

Date: 12, 2004 Sheet 33 of 50

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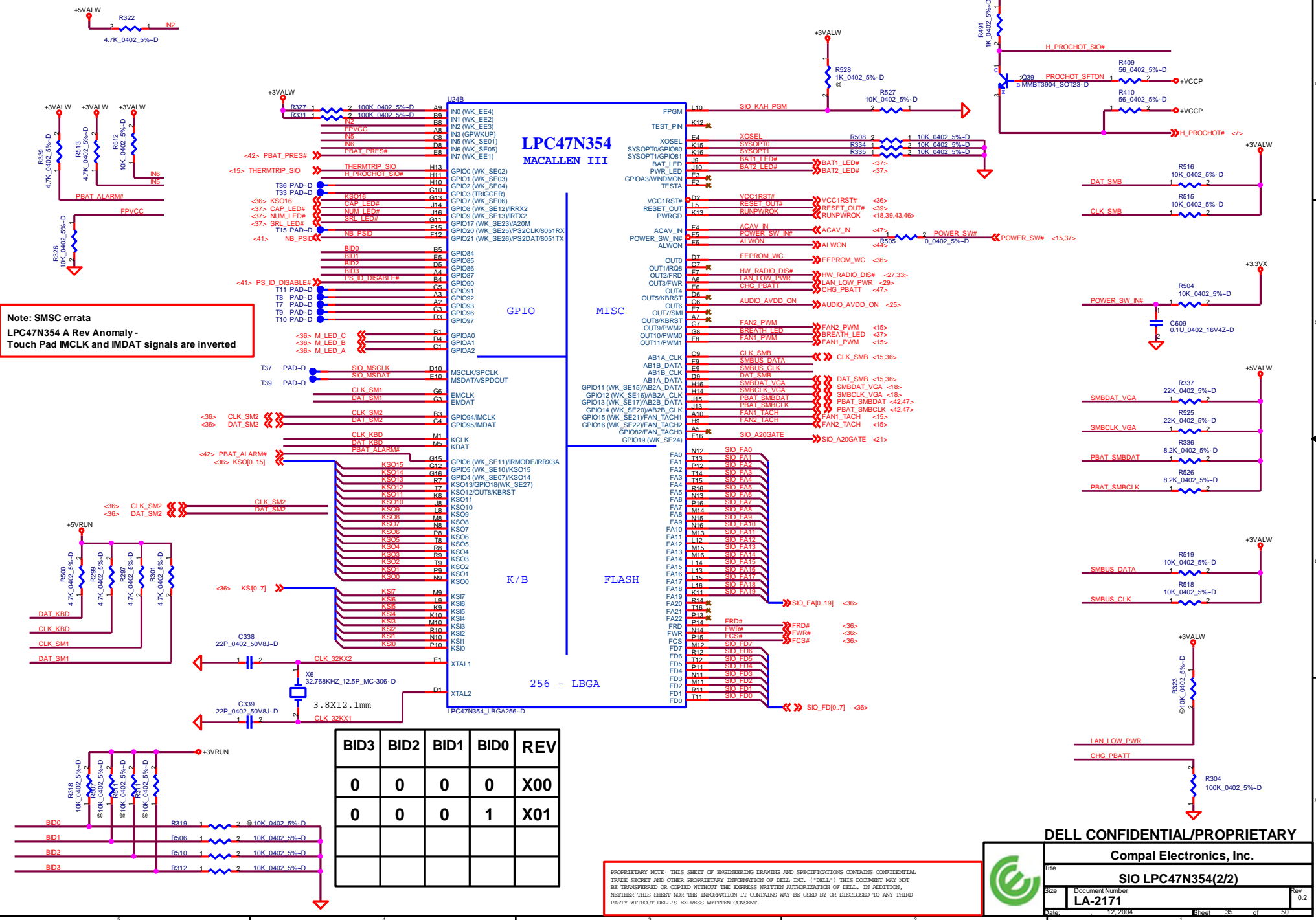
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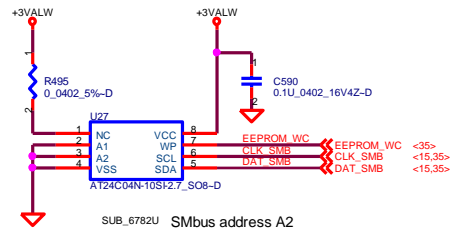
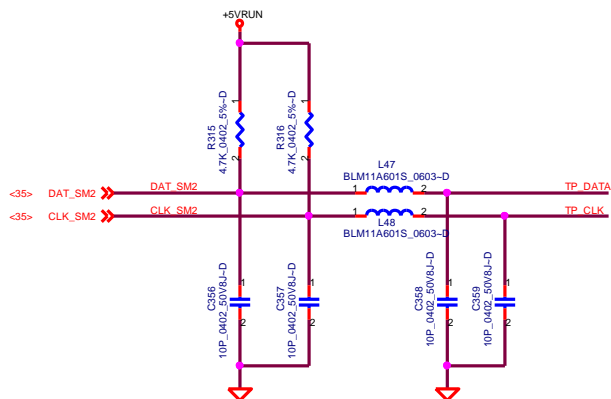
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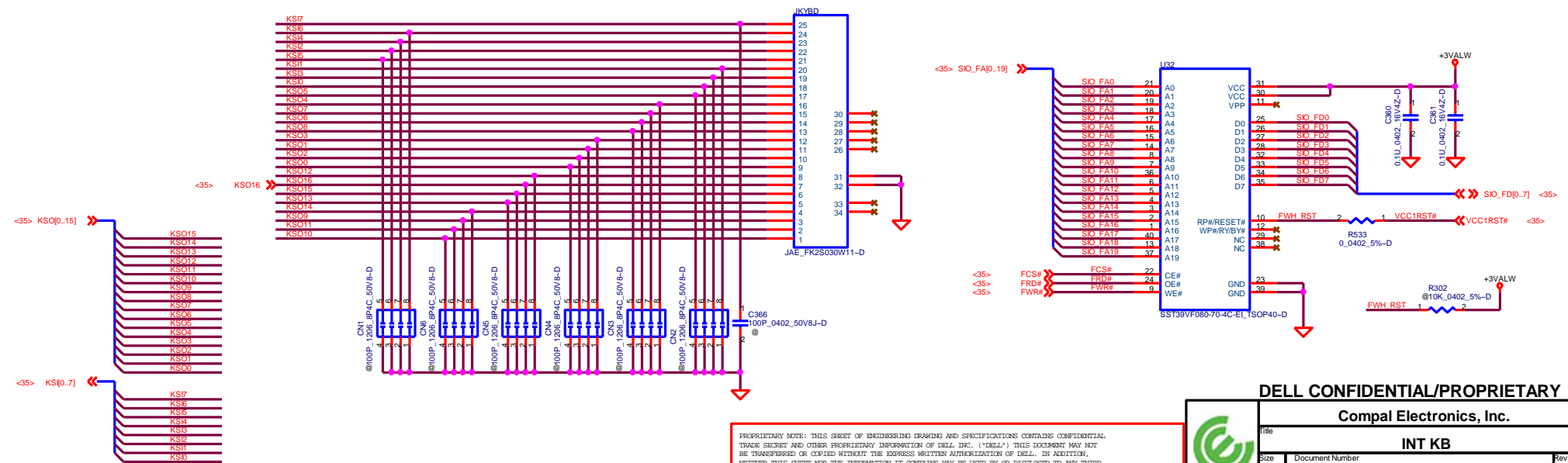
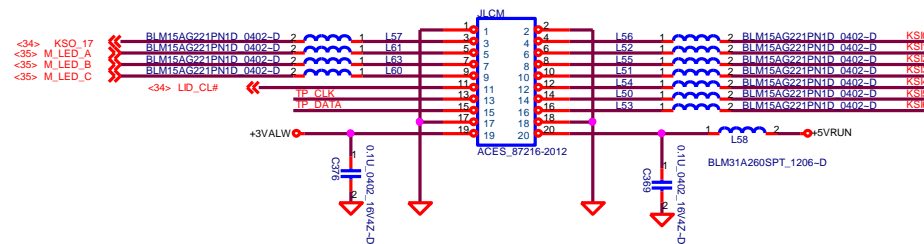
Size	Document Number	Rev
	<b>LA-2171</b>	0.1
Date:	12, 2004	Sheet 34 of 50

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## LCM &amp; Direct play SW &amp; T PAD



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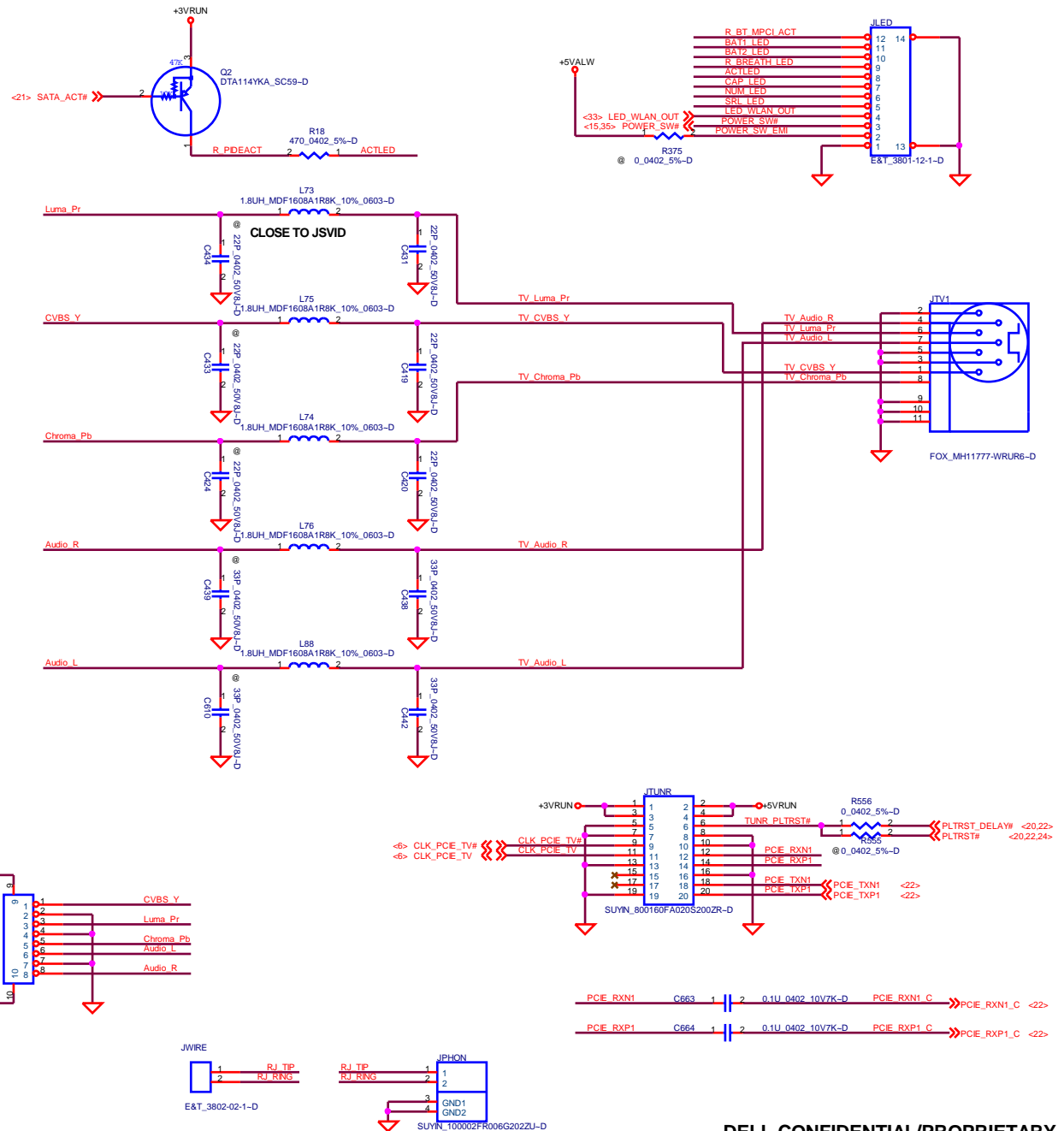


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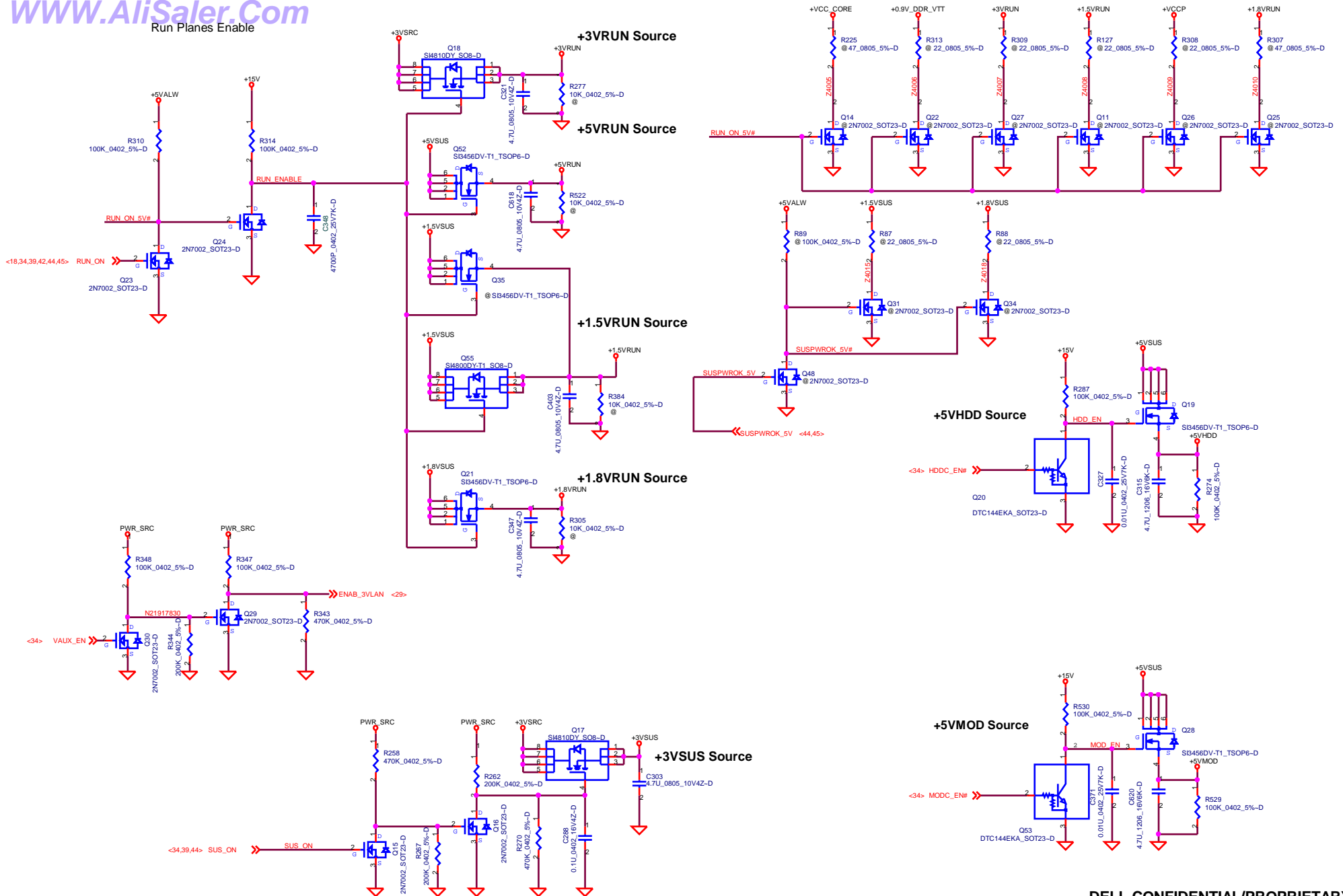
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Size	Document Number	Rev
	<b>LA-2171</b>	0.2
Date:	12/2004	Sheet 36 of 50



Size	Document Number	Rev
	<b>LA-2171</b>	0.2
Date:	12, 2004	Sheet 37 of 50



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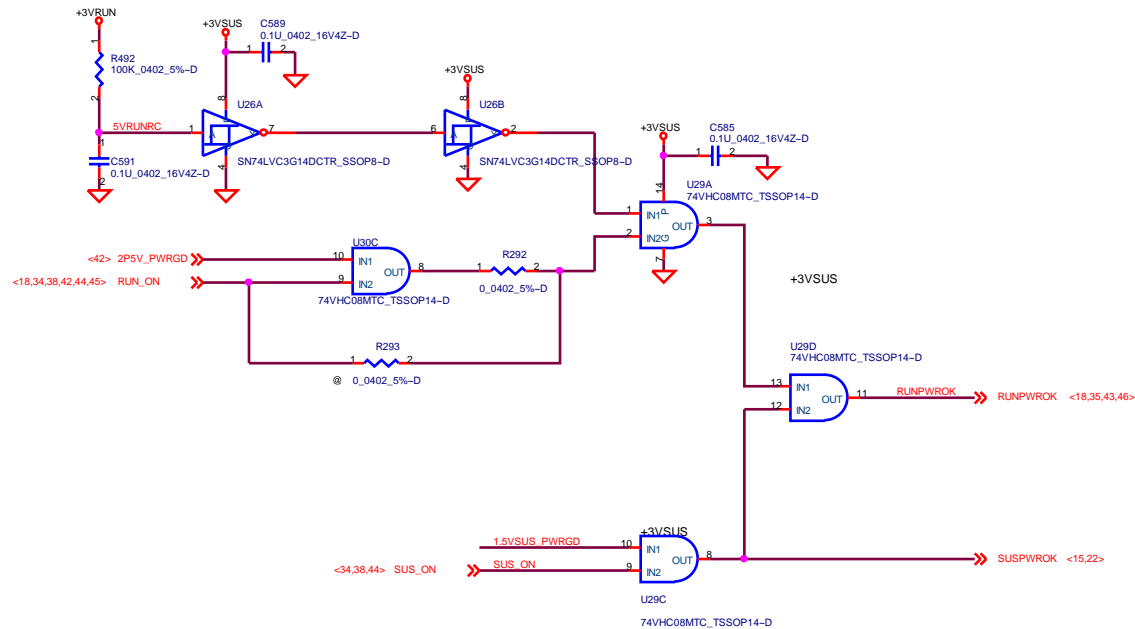
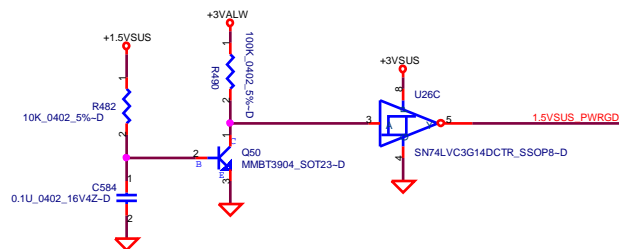
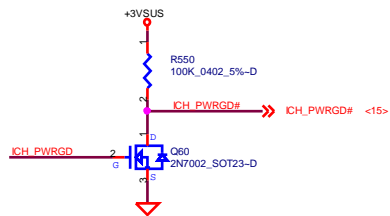
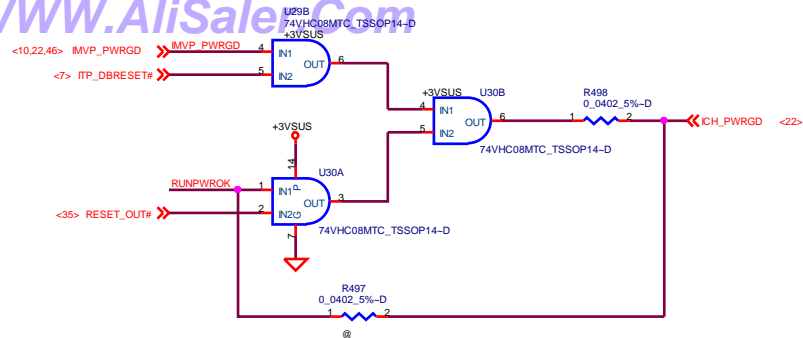
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POWER CONTROL

Size Document Number  
LA-2171

Date 12, 2004 Sheet 38 of 50

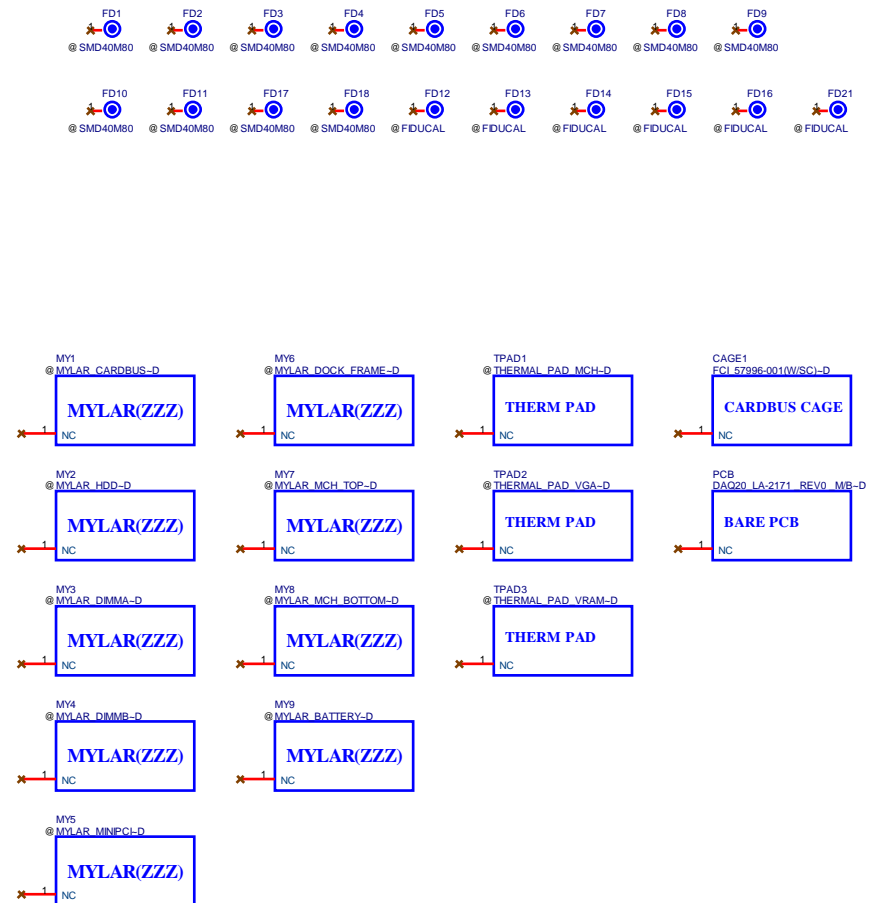
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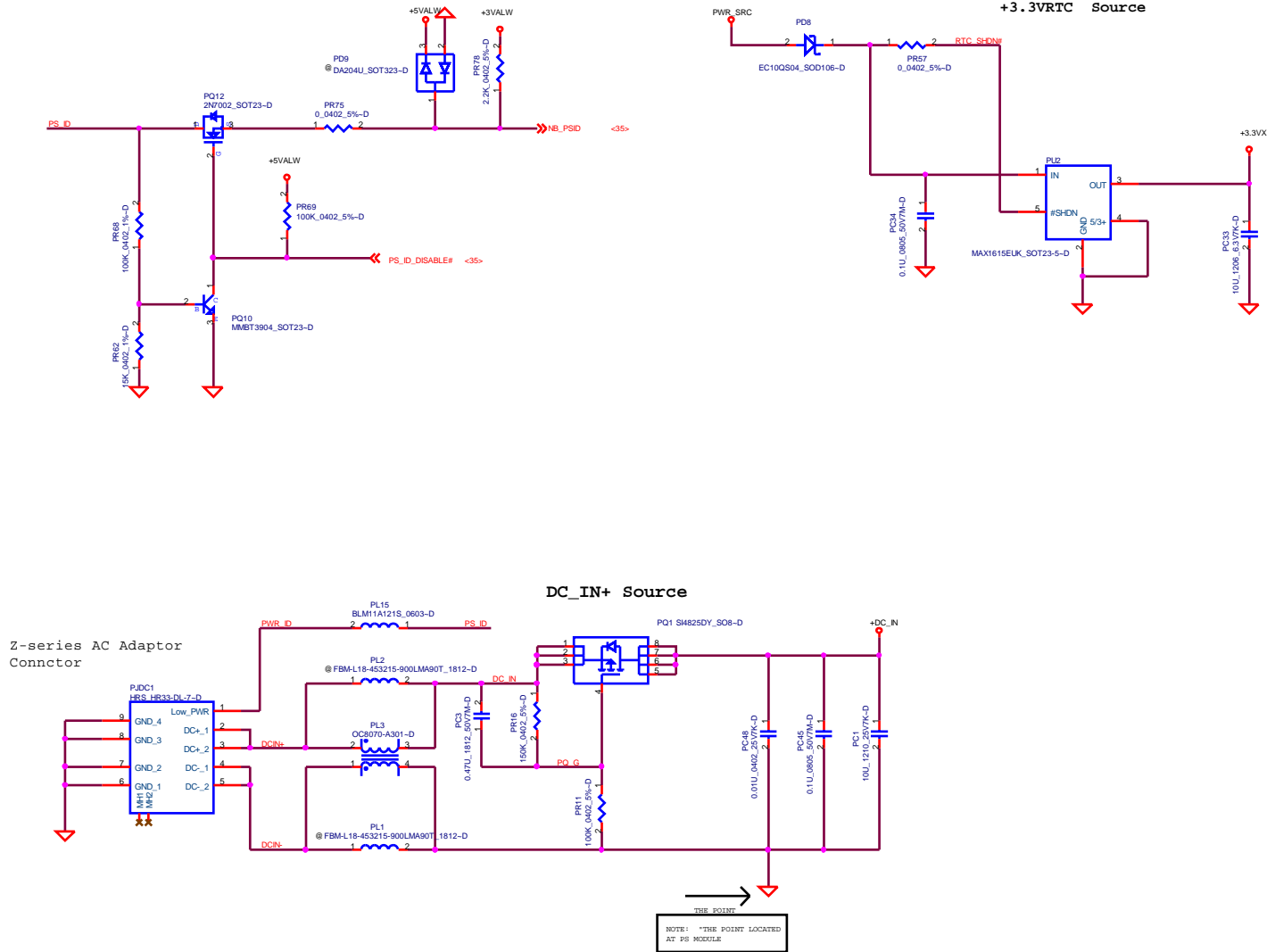


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Title		Power Good	
Size	Document Number	Rev	
	LA-2171	0.2	
Date	12, 2004	Sheet	39 of 50



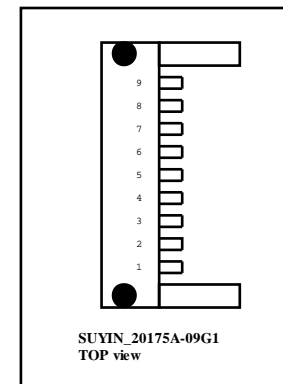
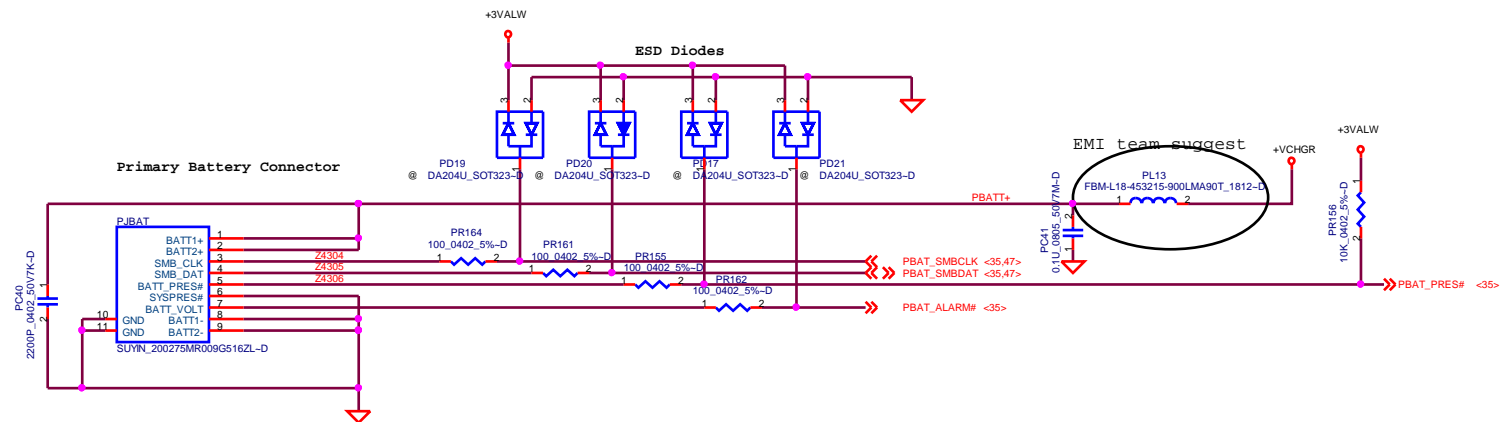
Size	Document Number	Rev
	LA-2171	0.2
Date:	12, 2004	Sheet 40 of 50

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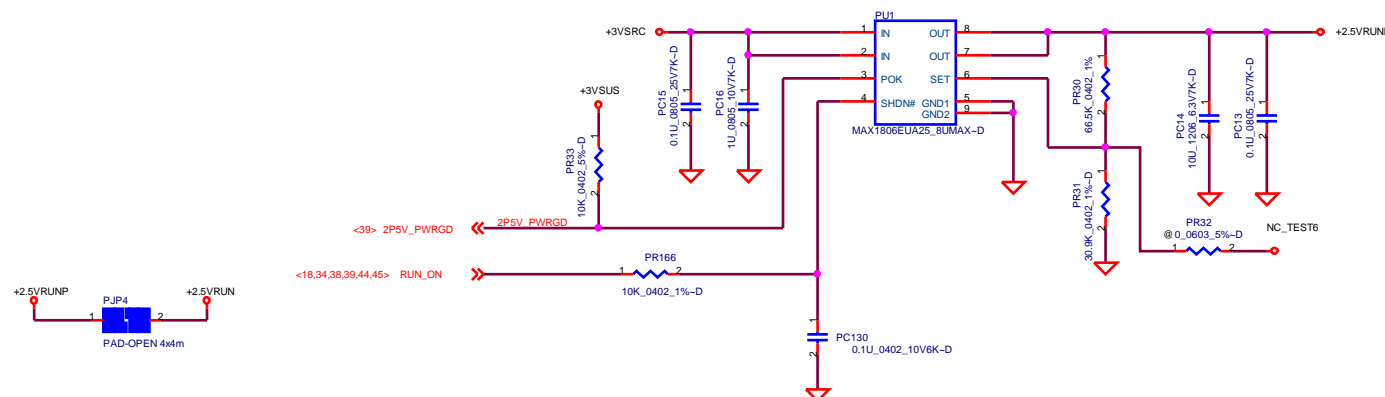
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+DCIN	
File	Document Number
LA-2171	Rev 0.2
Date	Sheet
12/2004	41 of 50



## +2.5V RUN

$$R1 = R2 * (V_o / 0.8 - 1), R2: 25K \sim 100K.$$



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Battery Conn./+2.5V

Document Number  
LA-2171

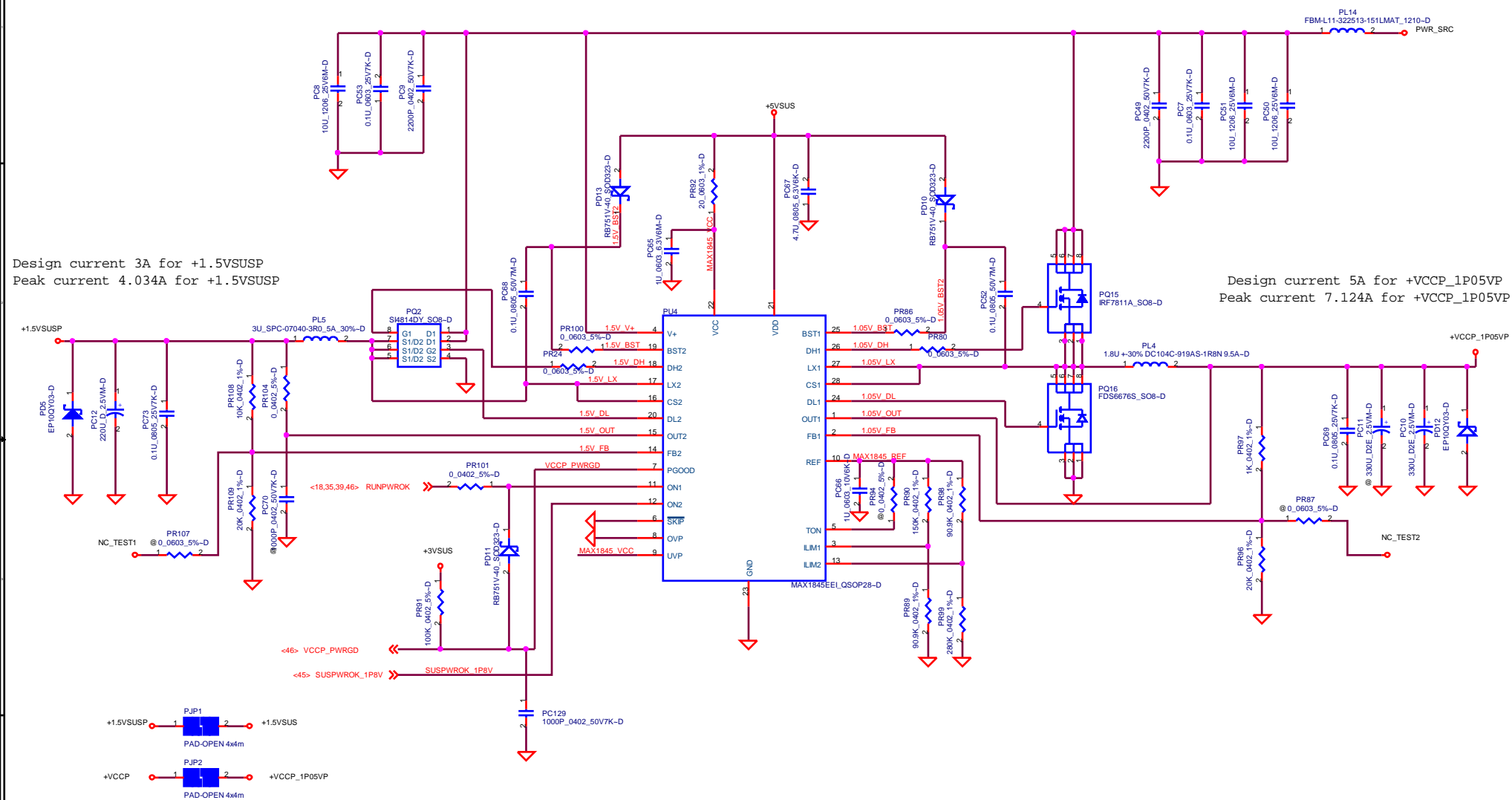
Rev  
0.2

Date: 12/2004 Sheet: 42 of 50

+1.5VSUSP / +VCCP\_1P05VP

Design current 3A for +1.5VSUSP  
Peak current 4.034A for +1.5VSUSP

Design current 5A for +VCCP\_1P05VP  
Peak current 7.124A for +VCCP\_1P05VP



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+1.5VSUSP /+VCCP\_1P05VP

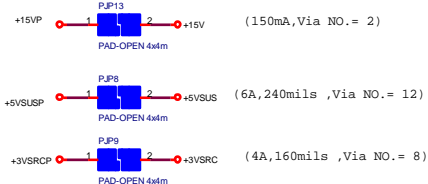
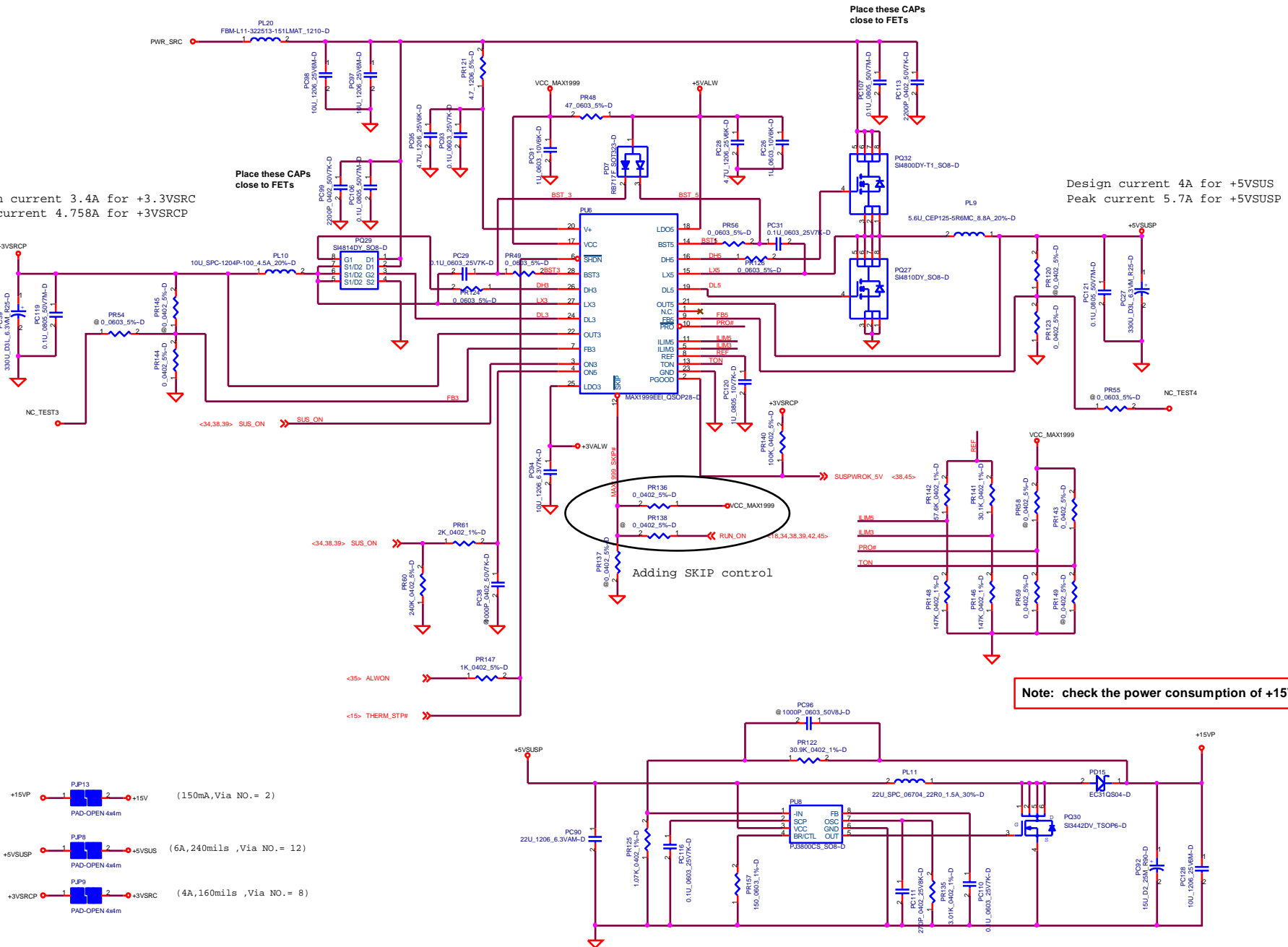
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Size: Document Number  
Rev: 0.2  
Date: 12/2004 Sheet: 43 of 50

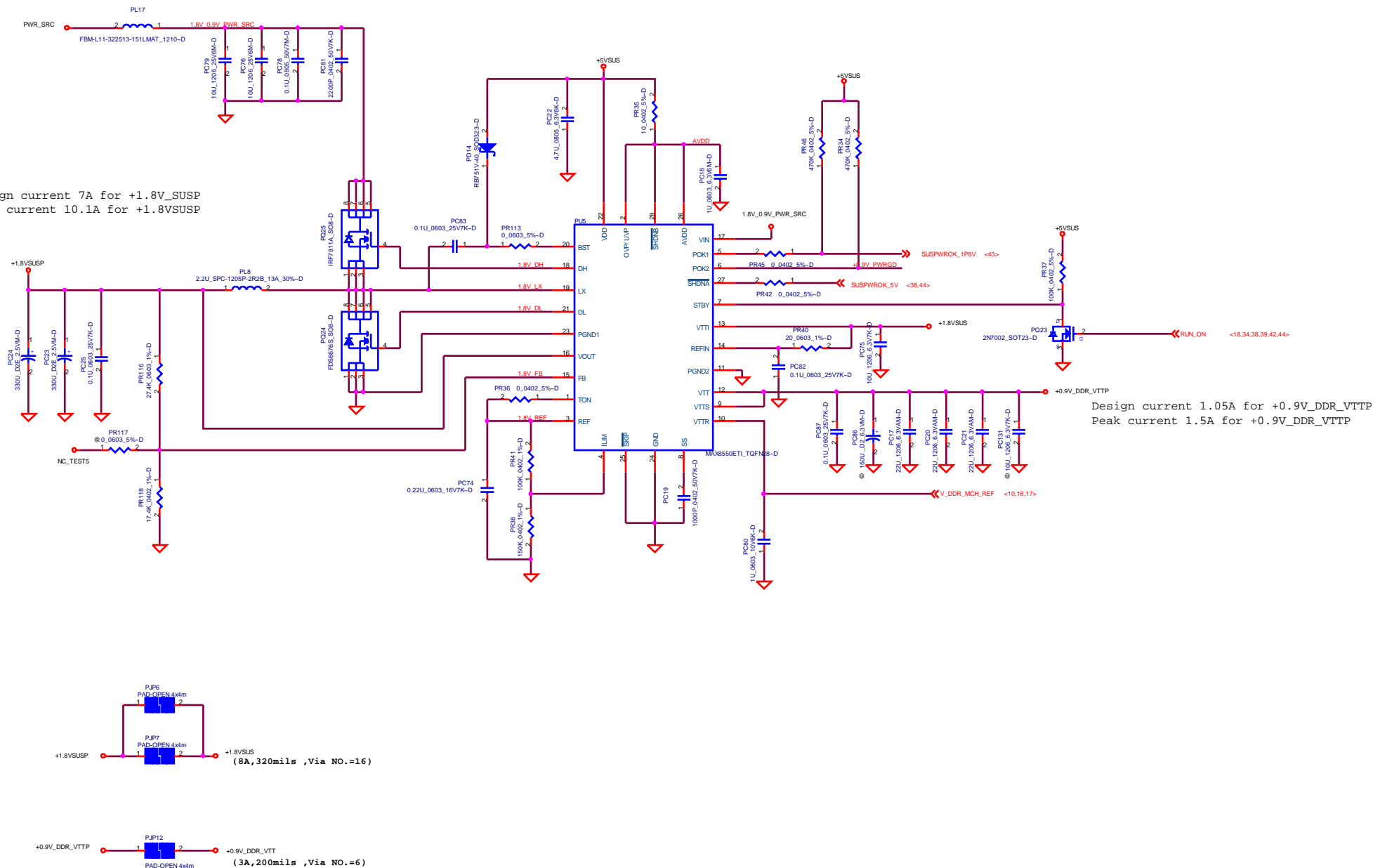
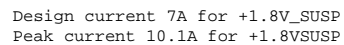
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DC/DC +3V/ +5V/ +15V

Design current 3.4A for +3.3VSRCP  
Peak current 4.758A for +3.3VSRCP

Design current 4A for +5VSUSP  
Peak current 5.7A for +5VSUSP



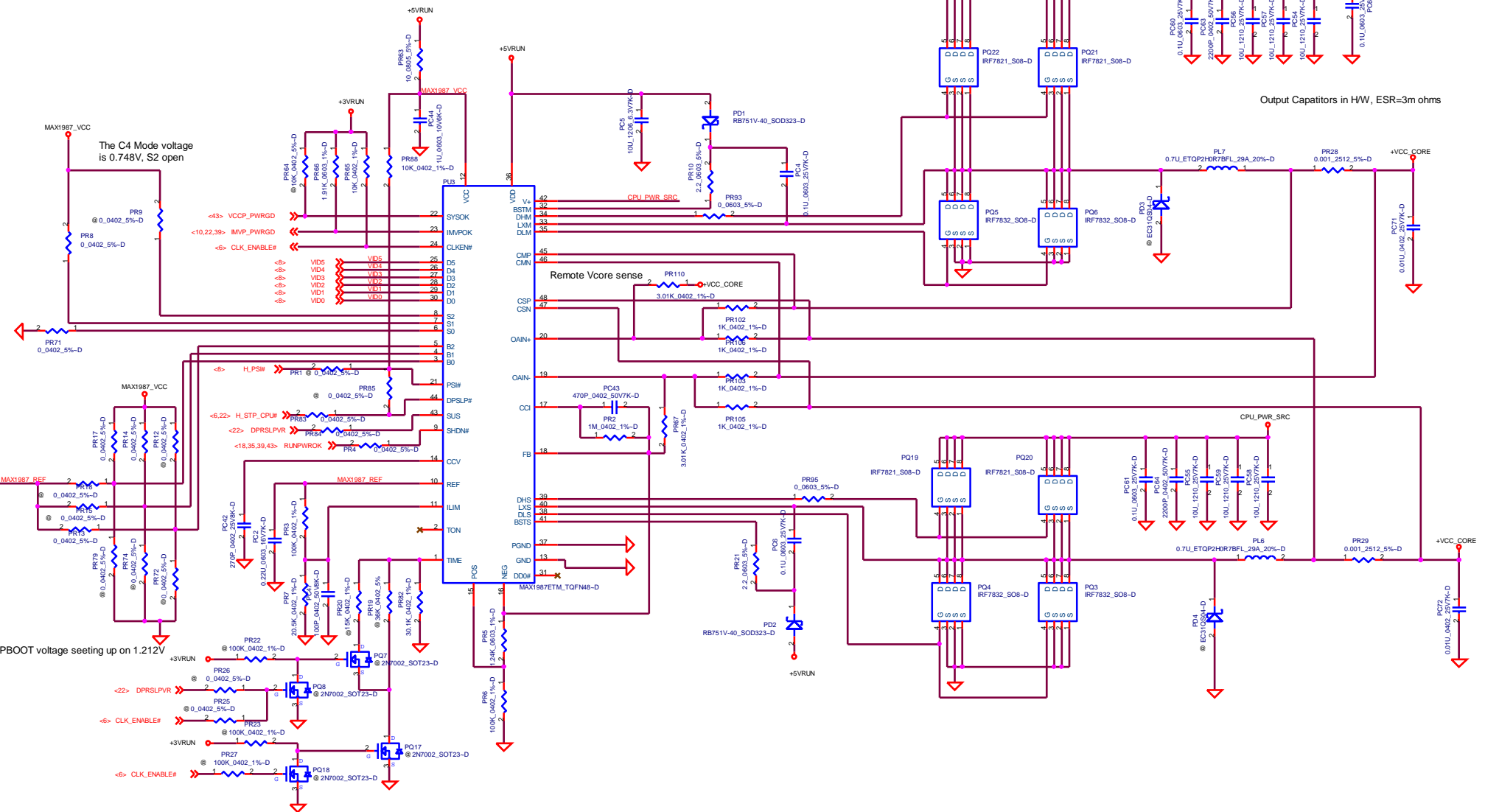


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DELL CONFIDENTIAL/PROPRIETARY			
Title +1.8VSUSP/ +0.9V_DDR_VT			
Size	Document Number Board Number LA2111		Rev 0.1
Issue	19_2000	Sheet 25 of 50	

VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Vcore
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.308
1	0	1	1	1	1	0.956
1	1	1	1	0	0	0.748



Change PR62-30 1k, Delete PR22/PO8/PQ17/PQ1/PQ18/PR20/PR26/PR23 and PR19 for BANIAS and DOTHAN  
 PR22/PQ8/PQ17/PQ1/PQ18/PR20/PR26/PR23 and PR19 are only for YONAH CPU.  
 TRANSITION TIMING:  
 (a): START-UP and SHUTDOWN (SUS=LOW, RUNPWROK=LOW): 2mV/us  
 (b): ENTER SUSPEND (SUS=HIGH, RUNPWROK=HIGH): 8.6mV/us  
 (c): EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH): 24.7mV/us

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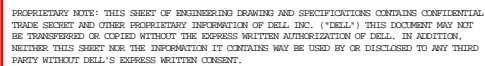
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+VCORE

Document Number LA-2171

Rev 0.2

Date 12-2004 Sheet 1 of 1



# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31&32	Cardbus	10/15/03	Dell	Change cardbus controller to TI PCI4515.	Change U162	M00
2	18	VGA/B & DVI CONN.	10/16/03	Dell	Add DVI connector.	Add JDVI	M00
3	25	SATA Bridge	10/16/03	Dell	Add SATA to PATA circuit.	Add page 25	M00
4	28	Subwoofer	10/16/03	Dell	Add subwoofer circuit.	Add page 28	M00
5	40	LED/B	10/16/03	Dell	Removed IR circuit.	Delete U52	M00
6	27	Amplifier & Phone JACK	10/17/03	Dell	Removed internal MIC circuit.		X00
7	31&32	LOM	10/17/03	Dell	Change LAN controller (U164) from 5751M to 4401. Add pop option for the 5705 like Kapalua/Lindbergh board.		X00
8	33	Cardbus	10/17/03	Dell	Depop 1394 choke, L142 and pop bypass resistors, R1025, R1026, R1027, R1028		X00
9	1	Cover page	10/17/03	Dell	Change schematic revision from M00 to X00.		X00
10	40	PAD & ME & spare parts	01/07/04	Compal	For EMI requirement.	Pop CLP4,5,10,11,13 and depop CLP18	X01
11	22	ICH6(3/4)	01/08/04	Dell	Connected PCIE channel 1 to TV-Tuner connector.	Delete T4,T5,T29,T30 and add C661,C662	X01
12	37	LED/B & TV TUNER	01/08/04	Dell	Connected TV tuner signals.	Add C663,C664	X01
13	40	PAD & ME & spare parts	01/08/04	Compal	Added ME standoff.	Pop H12,H13,H14,H17,H20,H21,H26,H27	X01
14	32	CardBus(2/2)	01/28/04		Fixed SD card issue.	The pin11 of JSD need to be connected to GND and pin 12 need to be connected to U17 pin b3.	X01
15	10	Alviso(1/5)	01/28/04	Dell			
16	6	Clock Generator	01/28/04	Dell			
17	7&10	Dothan(1/2) &Alviso(1/5)	01/28/04	Dell			
18							
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Changed-List History



Size	Document Number	Rev
	LA-2171	0.2

Date: 12/2004 Sheet 48 of 50

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Title  
Changed-List History  
Size Document Number Rev  
LA-2171 0.2  
Date: 12, 2004 Sheet 49 of 50

Version Change List (P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	Charger selector	2003/10/14	Compal	Modify charger selector circuit.	Need to discuss.	0.0
2	42	PSID & +3VX	2003/10/15	Compal	Modify PSID circuit same as Nimitas. And add current limit resistor on RTC charger.	Add ESD solution on PSID, and limit RTC charge current.	0.0
3	44	+15VP	2003/11/4	Compal	+15VP current rating is not enough for subwoofer	Use MB3800 Boost IC to genearte +15VP from +5VSUSP	X00
4	47	Charger	2003/11/5	Compal	That has leakage current from battery goes through PQ22 and PQ44 to DC_IN.	Move Adaptor current sense PR144 after PQ24 and before PWR_SRC. That is same as Nimitaz.	X00
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Power-Changed-List History

Size

Document Number

LA-2171

Rev

0.2

Date

12/2004

Sheet

50

of

50